

09/830963

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
 REQUEST FOR FILING NATIONAL PHASE OF
PCT APPLICATION UNDER 35 U.S.C. 371 AND 37 CFR 1.494 OR 1.495

To: Hon. Commissioner of Patents
 Washington, D.C. 20231



00909

TRANSMITTAL LETTER TO THE UNITED STATES
 DESIGNATED/ELECTED OFFICE (DO/EO/US)

Atty Dkt: P 280152 /7050P-U
 M# /Client Ref.

From: Pillsbury Winthrop LLP, IP Group:

Date: May 3, 2001

This is a **REQUEST** for **FILING** a PCT/USA National Phase Application based on:

1. International Application	2. International Filing Date	3. Earliest Priority Date Claimed
PCT/JP00/07037 <u>↑ country code</u>	10 October 2000 Day MONTH Year	26 October 1999 Day MONTH Year

(use item 2 if no earlier priority)

Measured from the earliest priority date in item 3, this PCT/USA National Phase Application Request is being filed within:

(a) 20 months from above item 3 date (b) 30 months from above item 3 date,
 (c) Therefore, the due date (unextendable) is June 26, 2001

5. Title of Invention MULTI-LAYER PRINTED CIRCUIT BOARD AND METHOD OF MANUFACTURING MULTI-LAYER PRINTED CIRCUIT BOARD

6. Inventor(s) KAWASAKI, Yogo et al

Applicant herewith submits the following under 35 U.S.C. 371 to effect filing:

7. Please immediately start national examination procedures (35 U.S.C. 371 (f)).

8. A copy of the International Application as filed (35 U.S.C. 371(c)(2)) is transmitted herewith (file if in English but, if in foreign language, file only if not transmitted to PTO by the International Bureau) including:

- Request;
- Abstract;
- ____ pgs. Spec. and Claims;
- ____ sheet(s) Drawing which are informal formal of size A4 11"

9. A copy of the International Application has been transmitted by the International Bureau.

10. A translation of the International Application into English (35 U.S.C. 371(c)(2))

- is transmitted herewith including: (1) Request; (2) Abstract;
 (3) 75 pgs. Spec. and Claims;
 (4) 22 sheet(s) Drawing which are:
 informal formal of size A4 11"
- is not required, as the application was filed in English.
- is not herewith, but will be filed when required by the forthcoming PTO Missing Requirements Notice per Rule 494(c) if box 4(a) is X'd or Rule 495(c) if box 4(b) is X'd.
- Translation verification attached (not required now).

11. Please see the attached Preliminary Amendment

12. Amendments to the claims of the International Application **under PCT Article 19 (35 U.S.C. 371(c)(3))**, i.e., before 18th month from first priority date above in item 3, are transmitted herewith (file only if in English) including:

13. PCT Article 19 claim amendments (if any) have been transmitted by the International Bureau

14. Translation of the amendments to the claims **under PCT Article 19 (35 U.S.C. 371(c)(3))**, i.e., of **claim amendments** made before 18th month, is attached (required by 20th month from the date in item 3 if box 4(a) above is X'd, or 30th month if box 4(b) is X'd, or else amendments will be considered canceled).

15. **A declaration of the inventor (35 U.S.C. 371(c)(4))**
 a. is submitted herewith Original Facsimile/Copy
 b. is not herewith, but will be filed when required by the forthcoming PTO Missing Requirements Notice per Rule 494(c) if box 4(a) is X'd or Rule 495(c) if box 4(b) is X'd.

16. **An International Search Report (ISR):**
 a. Was prepared by European Patent Office Japanese Patent Office Other
 b. has been transmitted by the international Bureau to PTO.
 c. copy herewith (pg(s)) plus Annex of family members (pg(s)).

17. **International Preliminary Examination Report (IPER):**
 a. has been transmitted (if this letter is filed after 28 months from date in item 3) in English by the International Bureau with Annexes (if any) in original language.
 b. copy herewith in English.
 c. 1 IPER Annex(es) in original language ("Annexes" are amendments made to claims/spec/drawings during Examination) including attached amended:
 c. 2 Specification/claim pages # claims #
 Dwg Sheets #
 d. Translation of Annex(es) to IPER (required by 30th month due date, or else annexed amendments will be considered canceled).

18. **Information Disclosure Statement** including:
 a. Attached Form PTO-1449 listing documents
 b. Attached copies of documents listed on Form PTO-1449
 c. A concise explanation of relevance of ISR references is given in the ISR.

19. **Assignment** document and Cover Sheet for recording are attached. Please mail the recorded assignment document back to the person whose signature, name and address appear at the end of this letter.

20. Copy of Power to IA agent.

21. **Drawings** (complete only if 8d or 10a(4) not completed): sheet(s) per set: 1 set informal; Formal of size A4 11"

22. Small Entity Status is Not claimed is claimed (pre-filing confirmation required)
 22(a) (No.) Small Entity Statement(s) enclosed (since 9/8/00 Small Entity Statements(s) not essential to make claim)

23. **Priority** is hereby claimed under 35 U.S.C. 119/365 based on the priority claim and the certified copy, both filed in the International Application during the international stage based on the filing in (country) JAPAN of:

<u>Application No.</u>	<u>Filing Date</u>	<u>Application No.</u>	<u>Filing Date</u>
(1) 11-303305	October 26, 1999	(2) 11-303306	October 26, 1999
(3) 11-303307	October 26, 1999	(4) 2000-029988	February 8, 2000
(5)		(6)	

a. See Form PCT/IB/304 sent to US/DO with copy of priority documents. If copy has not been received, please proceed promptly to obtain same from the IB.
 b. Copy of Form PCT/IB/304 attached.

RE: USA National Phase Filing of PCT/JP00/07037

JC08 Rec'd PCT/PTO 03 MAY 2001

24. Attached:

25 Per Item 17.c2, cancel original pages #_____, claims #_____, Drawing Sheets #_____,

26. **Calculation of the U.S. National Fee (35 U.S.C. 371 (c)(1)) and other fees is as follows:**
Based on amended claim(s) per above item(s) 12. 14. 17. 25 (hilite)

Total Effective Claims	minus 20 =	x \$18/\$9	= \$0	966/967
Independent Claims	minus 3 =	x \$80/\$40	= \$0	964/965
If any proper (ignore improper) Multiple Dependent claim is present,		add \$270/\$135	+0	968/969

BASIC NATIONAL FEE (37 CFR 1.492(a)(1)-(4)): ➤➤ BASIC FEE REQUIRED, NOW ➤➤➤➤

A. If country code letters in item 1 are not "US", "BR", "BB", "TT", "MX", "IL", "NZ", "IN" or "ZA"

See item 16 re:

1. Search Report was not prepared by EPO or JPO ----- add\$1000/\$500 960/961
2. Search Report was prepared by EPO or JPO ----- add\$860/\$430 +860 970/971

SKIP B, C, D AND E UNLESS country code letters in item 1 are "US", "BR", "BB", "TT", "MX", "IL", "NZ", "IN" or "ZA"

<input type="checkbox"/> B. If <u>USPTO</u> did not issue <u>both</u> International Search Report (ISR) <u>and</u> (if box 4(b) above is X'd) the International Examination Report (IPER), -----	add \$1000/\$500	+0	960/961
<input type="checkbox"/> C. If <u>USPTO</u> issued ISR but not IPER (or box 4(a) above is X'd), -----	add \$710/\$355	+0	958/959
<input type="checkbox"/> D. If <u>USPTO</u> issued IPER but IPER Sec. V boxes <u>not all</u> 3 YES, -----	add \$690/\$345	+0	956/957
<input type="checkbox"/> E. If international preliminary examination fee was paid to <u>USPTO</u> <u>and</u> Rules 492(a)(4) and 496(b) <u>satisfied</u> (IPER Sec. V <u>all</u> 3 boxes YES for <u>all</u> claims), -----	add \$100/\$50	+0	962/963

27.	SUBTOTAL =	<u>\$860</u>	
28.	If Assignment box 19 above is X'd, add Assignment Recording fee of ----\$40	<u>+0</u>	(581)
29.	Attached is a check to cover the -----	TOTAL FEES	\$860

Our Deposit Account No. 03-3975

Our Order No. 41226 280152
C# M#



00909

CHARGE STATEMENT: The Commissioner is hereby authorized to charge any fee specifically authorized hereafter, or any missing or insufficient fee(s) filed, or asserted to be filed, or which should have been filed herewith or concerning any paper filed hereafter, and which may be required under Rules 16-18 and 492 (missing or insufficient fee only) now or hereafter relative to this application and the resulting Official document under Rule 20, or credit any overpayment, to our Account/Order Nos. shown above for which purpose a duplicate copy of this sheet is attached.

This CHARGE STATEMENT does not authorize charge of the issue fee until/unless an issue fee transmittal form is filed.

**Pillsbury Winthrop LLP
Intellectual Property Group**

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Atty/Sec: gjp/mhn

NOTE: File in duplicate with 2 postcard receipts (PAT-103) & attachments.

09/830963

JC08 Rec'd PCT/PTO 03 MAY 2001

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re PATENT APPLICATION OF

Inventor(s): KAWASAKI, Yogo et al

Filed: Herewith

Title: MULTI-LAYER RINTED CIRCUIT BOARD AND METHOD OF MANUFACTURING
MULTI-LAYER PRINTED CIRCUIT BOARD

May 3, 2001

PRELIMINARY AMENDMENTHon. Commissioner of Patents
Washington, D.C. 20231

Sir:

Please amend this application as follows:

IN THE SPECIFICATION:

At the top of the first page, just under the title, insert

--This application is the National Phase of International Application
PCT/JP00/07037 filed October 10, 2000 which designated the U.S.
and that International Application
 was was not published under PCT Article 21(2) in English.--

Respectfully submitted,

PILLSBURY WINTHROP LLP
Intellectual Property GroupBy: 

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APPLICATION UNDER UNITED STATES PATENT LAWS

Atty. Dkt. No. PW 280152/7050P-U
(M#)

Invention: MULTI-LAYER PRINTED CIRCUIT BOARD AND METHOD OF MANUFACTURING MULTI-LAYER PRINTED CIRCUIT BOARD

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This is a:

- Provisional Application
- Regular Utility Application
- Continuing Application
 - The contents of the parent are incorporated by reference
- PCT National Phase Application
- Design Application
- Reissue Application
- Plant Application
- Substitute Specification
 - Sub. Spec Filed _____ / _____
in App. No. _____ / _____
- Marked up Specification re
Sub. Spec. filed _____ / _____
In App. No _____ / _____

SPECIFICATION

TITLE OF THE INVENTION

MULTI-LAYER PRINTED CIRCUIT BOARD AND METHOD OF MANUFACTURING
MULTI-LAYER PRINTED CIRCUIT BOARD

5 Technical Field

The present invention relates to a multi-layer printed circuit board having buildup layers formed on the both sides of a core substrate, the buildup layers each having interlayer resin insulating layers and conductor layers alternately provided, the conductor layers connected to one another by via holes. More particularly, the present invention relates to a multi-layer printed circuit board and a method of manufacturing a multi-layer printed circuit board which can be employed as a package substrate on which IC chips can be mounted.

15

Background Art

Hitherto, a buildup multi-layer printed circuit board has been manufactured by a method disclosed by, for example, Japanese Patent Laid-Open No. 9-130050.

20 A rough layer is formed on the surface of the conductor circuit of a printed circuit board by electroless plating or etching. Then, an interlayer insulating resin is applied, exposed and developed by a roll coater or printing, via hole opening portions are formed for making layers continuous, and
25 an interlayer resin insulating layer is formed through UV hardening, actual hardening and the like. Further, a catalyst such as palladium is applied onto the interlayer resin insulating

layer on the rough surface which has been subjected to a roughing process with an acid or an oxidizer. A thin electroless plated film is formed, a pattern is formed on the plated film by a dry film and the thickness of the pattern is increased by 5 electroplating. Thereafter, the dry film is separated and removed by an alkali and etched to thereby form a conductor circuit. By repeating the above processes, a buildup multi-layer printed circuit board is obtained.

At present, as the frequency of IC chips becomes higher, 10 demand for accelerating the transmission speed of a multi-layer printed circuit board rises. To deal with such demand, the applicant of the present invention proposed Japanese Patent Laid-Open No. 10-334499. With this constitution, linear wirings are provided by arranging via holes 346 of a lower 15 interlayer resin insulating layer 350 and via holes 366 of an upper interlayer resin insulating layer 360 right above through holes 336, thereby shortening wiring lengths and accelerating signal transmission speed.

It was discovered, however, that with the above 20 constitution, the via holes 346 of the lower interlayer resin insulating layer 350 and the via holes 366 of the upper interlayer resin insulating layer 360 are separated from one another under heat cycle conditions. The inventor of the present invention investigated the cause of separation and discovered that the 25 via holes 366 in the upper layer are influenced by the shapes of the surfaces of the via holes 346 of the lower layer and the connection characteristic of the via holes 366 deteriorates.

Further, it is estimated that since the interlayer resin insulating layers 350 and 360 are not reinforced by core materials such as glass cloth, these layers tend to be separated in a heat cycle rather than a core substrate provided with a core material.

5 The present invention has been made to overcome the foregoing problems, and it is, therefore, an object of the present invention to provide a multi-layer printed circuit board and a method of manufacturing a multi-layer printed circuit board capable of shortening internal wiring lengths and having
10 excellent connection reliability.

It is a still further object of the present invention to provide a manufacturing method capable of manufacturing a multi-layer printed circuit board at low cost.

Meanwhile, a resin is filled in through holes so as to
15 enhance reliability for a buildup multi-layer printed circuit board. When filling the resin, blackening-reduction processes are conducted to the surfaces of the through holes and rough layers are provided thereon so as to increase adhesiveness. In addition, as the density of the multi-layer printed circuit board
20 increases, through holes are made smaller in size. Following this, resin filler having low viscosity is employed to be filled in the through holes.

As prior art for forming a rough layer on a through hole and filling the through hole with resin filler, it is described
25 in Japanese Patent Laid-Open No. 9-181415 that a copper oxide layer is formed in a through hole, the through hole is filled with resin filler and then an interlayer insulating layer is

formed. It is also described in Japanese Patent Laid-Open No. 9-260849 that after forming a rough layer in a through hole by etching, the through hole is filled with resin filler and then an interlayer insulating layer is formed.

5 If using resin filler having low viscosity, however, the resin filler is dented in the through hole, causing disconnection and the like during the formation of wirings on an upper layer. The inventor of the present invention investigated the cause of disconnection and discovered that this is because the resin 10 out of filler and the resin which constitute resin filler flow along the rough layer (very small anchor) formed on the land of the through hole. As a result, the filler within the through hole is dented, making it impossible to flatten and smooth a core substrate. Due to this, it was discovered that if 15 manufacturing a multi-layer printed circuit board by forming an interlayer resin insulating layer and wirings on a core substrate, the resultant multi-layer resin insulating layer is susceptible to disconnection and a probability of generating defects increases.

20 The present invention has been made to solve the foregoing problems and it is, therefore, a still further object of the present invention to provide a method of manufacturing a multi-layer printed circuit board having enhanced wiring reliability.

25 In the meantime, a substrate on which a resin film for the interlayer resin insulating layer of a resin substrate serving as a core material is bonded, is employed as a core

substrate. Through holes for penetrating the substrate are filled with resin filler. Further, an interlayer resin insulating layer is formed and via holes are formed therein. The above-stated resin filler, however, had some defects.

5 First, if a reliability test such as a heat cycle is conducted to a printed circuit board filled with filler, conductors sometimes crack in the vicinity of the boundary between the resin substrate and the resin film. Second, after filling the filler, a resin film serving as an interlayer resin 10 insulating layer cracks in a polishing step conducted to flatten the board. Third, if a plated cover is formed right on the through hole, the reaction of the plated film may stop. Thus, even if via holes are formed right above the through holes, electrical connection cannot be established.

15 As a result of these three defects, a printed circuit board with deteriorated reliability and reduced electrical connection characteristics is provided.

It is a still further object of the present invention to provide a printed circuit board and a method of manufacturing 20 a printed circuit board capable of solving these defects.

Disclosure of the Invention

In order to solve the above problems, a multi-layer printed circuit board according to the claim 1 is characterized by having 25 buildup layers formed on both sides of a core substrate, the buildup layers each having interlayer resin insulating layers and conductive layers alternately provided, the conductor layers

connected to one another by via holes, wherein
through holes are formed to penetrate said core substrate
and the interlayer resin insulating layers formed on the both
sides of the core substrate; and

5 the via holes are formed right on said through holes, the
via holes connected to external connection terminals.

In claim 2, A multi-layer printed circuit board according
to claim 1, wherein

10 resin filler is filled in said through holes and the
conductor layers are formed to cover exposed surfaces of the
resin filler from the through holes; and

the via holes right on said through holes are formed on
said conductor layers of said through holes.

According to claim 3, a method of manufacturing a
15 multi-layer printed circuit board comprising at least the
following steps (a) to (d):

(a) forming lower interlayer resin insulating layers
on both sides of a core substrate, respectively;

20 (b) forming through holes penetrating said core
substrate and said lower interlayer resin insulating layers;

(c) forming upper interlayer resin insulating layers
on said lower interlayer resin insulating layers, respectively;
and

25 (d) forming via holes in said upper interlayer resin
insulating layers, the via holes connected to external connection
terminals and formed right on part of said through holes.

According to claim 4, a method of manufacturing a

multi-layer printed circuit board comprising at least the following steps (a) to (g):

- (a) forming lower interlayer resin insulating layers on both sides of a core substrate, respectively;
- 5 (b) forming through holes penetrating said core substrate and said lower interlayer resin insulating layers;
- (c) filling resin filler in said through holes;
- (d) polishing and flattening the resin filler pouring from said through holes;
- 10 (e) forming conductor layers covering exposed surfaces of said resin filer from said through holes;
- (f) forming upper interlayer resin insulating layers on said lower interlayer resin insulating layers, respectively; and
- 15 (g) forming via holes in said upper interlayer resin insulating layers and forming the via holes right on part of said through holes so as to be connected to external connection terminals.

According to the multi-layer printed circuit board recited in claim 1 and the method of manufacturing the multi-layer printed circuit board recited in claim 3, the through holes are formed to penetrate the core substrate and the interlayer resin insulating layers formed on the both sides of the core substrate, and the via holes connected to external connection terminals are formed right on the through holes, respectively. Due to this, the through holes and the via holes are arranged linearly, thereby making it possible to shorten wiring length and

accelerate signal transmission speed. Further, since the through holes and the via holes connected to the external connection terminals are directly connected to one another, connection reliability is excellent.

5 According to the multi-layer printed circuit board recited in claim 2 and the method of manufacturing the multi-layer printed circuit board recited in claim 4, the through holes are formed to penetrate the core substrate and the interlayer resin insulating layers formed on the both sides of the core substrate, 10 and the via holes are formed right on the through holes, respectively. Due to this, the through holes and the via holes are arranged linearly, thereby making it possible to shorten wiring length and accelerate signal transmission speed. Further, since the through holes and the via holes connected 15 to the external connection terminals are directly connected to one another and the via holes are formed on the respective conductor layers covering the resin filler in the through holes which filler has been flattened by polishing, connection reliability is excellent.

20 According to claim 5, a multi-layer printed circuit board having interlayer resin insulating layers on both sides of a core substrate, respectively, through holes provided to penetrate the core substrate and filled with resin filler, the interlayer resin insulating layers and conductor circuits 25 provided, wherein

 said resin filler contains an epoxy resin, a curing agent and 10 to 50% of inorganic particles.

According to claim 6, a multi-layer printed circuit board having interlayer resin insulating layers formed on both sides of a core substrate, respectively, through holes provided to penetrate the core substrate and filled with resin filler, plated 5 covers provided, the interlayer resin insulating layers and conductor circuits provided, wherein

 said resin filler contains an epoxy resin, a curing agent and 10 to 50% of inorganic particles.

According to claim 7, a multi-layer printed circuit board 10 according to claim 5 or 6, wherein

 said inorganic particles contain one type or more selected from a group consisting of aluminum compounds, calcium compounds, potassium compounds, magnesium compounds and silicon compounds.

First, since the quantity of the mixed inorganic particles 15 is set appropriately, the coefficient of thermal expansion of the resin filler, that of the resin substrate forming the core substrate and those of the resin films for the interlayer resin insulating layers are matched to one another. Due to this, even on heat cycle conditions, a stress caused by heat contraction 20 does not occur. Thus, cracking does not occur. Further, the resin films are impregnated with soluble particles for forming rough surfaces by a roughing process. Due to this, it was discovered that if the quantity of mixed inorganic particles exceeds 50%, the matching cannot be ensured.

25 Second, it was discovered that in the polishing step conducted to flatten the filler after the filler is filled, the filler can be easily polished. It was discovered that if the

quantity of mixed inorganic particles exceeds 50%, the filler can be flattened only by mechanical polishing using abrasive paper. The resin films on the surface layers of the core substrate are not impregnated with a reinforcing material such 5 as glass epoxy and inferior, in strength, to the resin substrate. Due to this, if mechanical polishing with abrasive paper (such as belt sander polishing) is conducted, the resin films cannot resist the polishing. As a result, the resin films crack. Besides, the resin films are damaged, thereby detaching soluble 10 particles. Consequently, even if the rough surfaces are formed, they are not what are desired. Considering this, if a polishing process is performed, the surface layers of the core substrate are traced with a nonwoven fabric containing a polishing material such as a buff, thereby removing and flattening the resin filler.

15 Third, it was discovered that in the formation of plated covers right on the respective through holes, if an inorganic particle content exceeds 50%, the quantity of added catalyst decreases and the reaction of the plated films stops. The coordinate bond between the inorganic particles and the catalyst 20 does not occur. The quantity of added catalyst, therefore, decreases. Further, in the formation of the plated films, if the quantity of inorganic particles is excessive, a plating solution tends not to be contacted, thereby stopping the reaction of the plated films.

25 If the quantity of mixed inorganic particles is less than 10%, the effect of matching the coefficients of thermal expansion is not expected. As a result, if the resin filler is filled,

the resin filler is not left in the through holes and flows away from the other side.

It is more preferable that the mixture ratio of inorganic particles is 20 to 40%. In that range, even if particles 5 flocculate, the above-stated defects can be avoided.

According to claim 8, a multi-layer printed circuit board according to claim 5 or 6, wherein

a shape of said inorganic particles is one of a spherical shape, a circular shape, an ellipsoidal shape, a pulverized shape 10 and a polygonal shape.

Preferably, the particles are circular, ellipsoidal or the like without angular surfaces. This is because cracks resulting from such particles do not occur. It is also preferable that the particle diameter of the inorganic particles is in a range of 0.01 to 5 μm . If the particle diameter is less than 15 0.01 μm , the particles are offset one another when the resin filler is filled. If exceeding 5 μm , it is often difficult to adjust the mixture ratio of the inorganic particles in the resin.

In claim 9, a multi-layer printed circuit board according 20 to claim 5 and claim 6, wherein

rough layers are provided on the conductor layers of said through holes, respectively.

It is preferable that rough layers are provided on the conductor layers of the through holes, respectively. By doing 25 so, it is possible to prevent the resin filler from expanding and contracting, whereby the interlayer resin insulating layers and the plated covers formed on the respective through holes

are not pushed up. The rough layers are formed by an oxidization-reduction process, a blackening process or a plating process as well as by an etching process.

According to claim 10, a method of manufacturing a
5 multi-layer printed circuit board having interlayer resin insulating layers provided on both sides of a core substrate, for forming the interlayer resin insulating layers through the following steps (a) to (e):

- (a) a formation step of forming through holes
10 penetrating the both sides of the printed circuit board;
- (b) a filling step of filling resin filler containing an epoxy resin and 10 to 50% of inorganic particles;
- (c) a drying step and a polishing step;
- (d) a hardening step; and
15
- (e) a cover plating step.

In claim 11, a method according to claim 10, wherein in said polishing step (c), a buffering step is conducted at least once or a plurality of times.

In claim 12, a method according to claim 10 or 11, wherein
20 in said step (a), a step of forming rough layers is conducted.

In order to achieve the above problems, in claim 13, a multi-layer printed circuit board having buildup layers on both sides of a core substrate, respectively, said buildup layer
25 having interlayer resin insulating layers and conductor layers alternately provided, the conductor layers connected to one another by via holes, wherein

through holes filled with resin filler are formed to penetrate said core substrate and lower interlayer resin insulating layers formed on the both sides of the core substrate; and

5 via holes filled with said resin filler are formed in said lower interlayer resin insulating layers.

In case of the multi-layer printed circuit board recited in claim 13, the through holes and the via holes are filled with the same resin filler. Due to this, the multi-layer printed 10 circuit board can be manufactured at low cost and the strength within the through holes and that within the via holes can be kept uniform, thereby making it possible to enhance the reliability of the multi-layer printed circuit board.

The resin may be a thermosetting resin which means an epoxy 15 resin, a phenol resin, a fluorocarbon resin, a triazine resin, a polyolefin resin, a polyphenylene ether resin and the like, a thermoplastic resin or a complex thereof. Inorganic filler, such as silica or alumina, may be contained in the resin to adjust the coefficient of thermal expansion of the resin. A paste mainly 20 consisting of metal filler such as a conductive resin, gold or silver may be employed. The complexes thereof may be employed, as well.

In claim 14, a multi-layer printed circuit board according to claim 13, wherein

25 the conductor layers are formed to cover exposed surfaces of the resin filler filled in the via holes of said lower interlayer resin insulating layers; and

via holes are formed right on the via holes through the conductive layers, respectively.

According to claim 14, the conductor layers covering the exposed surfaces of the filler filled in the via holes of the 5 lower interlayer resin insulating layers are formed and the via holes are formed right on the via holes through the conductor layers, respectively. Due to this, the lower via holes can be formed flat and the adhesiveness between the lower via holes and the via holes formed on the corresponding via holes can be 10 enhanced to thereby enhance the reliability of the multi-layer printed circuit board.

According to claim 15, a method of manufacturing a multi-layer printed circuit board comprising at least the following steps (a) to (g):

15 (a) forming lower interlayer resin insulating layers on both sides of a core substrate, respectively;

(b) forming penetrating holes in said core substrate and said lower interlayer resin insulating layers, the penetrating holes becoming through holes;

20 (c) forming openings in said lower interlayer resin insulating layers, the openings becoming via holes;

(d) forming conductive films in said penetrating holes and said openings to thereby provide the through holes and the via holes, respectively;

25 (e) filling resin filler in said through holes and said via holes;

(f) polishing and flattening the resin filler pouring

out of said through holes and said via holes; and

(g) forming conductor layers covering exposed surfaces of said resin filler from said through holes and said via holes, respectively.

5 According to claim 16, a method of manufacturing a multi-layer printed circuit board comprising at least the following steps (a) to (i):

(a) forming lower interlayer resin insulating layers on both sides of a core substrate, respectively;

10 (b) forming penetrating holes in said core substrate and said lower interlayer resin insulating layers, the penetrating holes becoming through holes;

(c) forming openings in said lower interlayer resin insulating layers, the openings becoming via holes;

15 (d) forming conductive films in said penetrating holes and said openings to provide the through holes and the via holes;

(e) filling resin filler in said through holes and said via holes;

(f) polishing and flattening the resin filler pouring 20 out of said through holes and said via holes;

(g) forming conductor layers covering exposed surfaces of said resin filler from said through holes and said via holes;

(h) forming upper interlayer resin insulating layers on said lower interlayer resin insulating layers, respectively;

25 and

(i) forming via holes in said upper interlayer resin insulating layers and right on part of said via holes.

According to the method of manufacturing the multi-layer printed circuit board recited in claims 15 and 16, the same resin filler is filled in the through holes and the via holes and polished simultaneously. Due to this, the multi-layer printed circuit board can be manufactured at low cost and the strength within the through holes and that within the via holes can be kept uniform, so that the reliability of the multi-layer printed circuit board can be enhanced. Further, since the upper via holes are formed on the conductor layers covering the filler within the via holes which filler has been polished and thereby flattened, respectively, connection reliability is excellent.

In order to achieve the above problems, according to claim 17, a method of manufacturing a multi-layer printed circuit board comprising at least the following steps (a) to (e):

- 15 (a) forming lower interlayer resin insulating layers on both sides of a core substrate, respectively;
- (b) forming penetrating holes in said core substrate and said lower interlayer resin insulating layers, the penetrating holes becoming through holes;
- 20 (c) forming openings in said lower interlayer resin insulating layers, the openings becoming via holes;
- (d) conducting a de-smear process to said penetrating holes by an acid or an oxidizer and conducting a roughing process to surfaces of the lower interlayer resin insulating layers;
- 25 and
- (e) forming conductive films on said penetrating holes and said openings to provide the through holes and the via holes,

respectively.

According to the method of manufacturing the multi-layer printed circuit board recited in claim 17, the de-smear process for the penetrating holes by employing an oxidizer and the 5 roughing process for the surfaces of the lower interlayer resin insulating layers are performed simultaneously. Due to this, it is possible to reduce the number of manufacturing steps and to manufacture the multi-layer printed circuit board at low cost.

In claim 18, a method according to claim 17, wherein 10 said core substrate is made of one of a glass epoxy resin, an FR4 resin, an FR5 resin and a BT resin;

each of said lower interlayer resin insulating layers contains at least one of an epoxy resin, a phenol resin, a polyimide resin, a polyphenylene resin, a polyolefin resin and a 15 fluorocarbon resin; and

said oxidizer contains one of a chromic acid and permanganate.

According to claim 18, the core substrate is made of one of a glass epoxy resin, a FR4 resin, a FR5 resin and a BT resin. 20 Each of the lower interlayer resin insulating layers contains at least one of an epoxy resin, a phenol resin, a polyimide resin, a polyphenylene resin, a polyolefin resin and a fluorocarbon resin. The oxidizer contains one of a chromic acid and permanganate. Due to this, it is possible to simultaneously 25 perform the de-smear process for the penetrating holes for forming the lower interlayer resin insulating layers on the core substrate and the roughing process for the lower interlayer resin

insulating layers.

In order to achieve the above problems, according to claim 21, a method of manufacturing a multi-layer printed circuit board comprising at least the following steps (a) to (d):

- 5 (a) forming through holes in a core substrate;
- (b) forming rough layers on said through holes, respectively;
- (c) polishing and flattening surfaces of lands of said through holes; and
- 10 (d) filling resin filler in said through holes and forming resin layers.

According to claim 21, after forming the rough layers on the through holes, respectively, the surfaces of the lands of the through holes are polished and flattened. By doing so, it is possible to prevent the resin filler from flowing out along the rough layers (anchors) formed on the lands of the through holes when filling the resin filler in the through holes. Thus, it is possible to smoothly form the filler in the through holes and to enhance the reliability of wirings formed above the through holes.

In claim 22, a method according to claim 21, wherein said rough layers are copper oxide layers.

In claim 23, a method according to claim 21, wherein said rough layers are formed by etching.

25 In claim 24, a method according to claim 21, wherein said rough layers are needle alloy layers made of copper-nickel-phosphorous.

According to claims 22, 23 and 24, the rough layer formed on each through hole is preferably formed by one of the formation of a copper oxide layer by a blackening-reduction process, the formation of a needle alloy layer consisting of copper-nickel-phosphorous and by etching. By doing so, it is possible to enhance the adhesiveness between the conductor layers on the inner walls of the through holes and the resin filler.

In claim 25, a method according to claims 21, wherein said resin filler is one selected from a group consisting of a mixture of an epoxy resin and organic filler, a mixture of an epoxy resin and inorganic filler and a mixture of an epoxy resin and inorganic fiber.

According to claim 25, the resin filler to be employed is preferably one selected from a group consisting of a mixture of an epoxy resin and organic filler, a mixture of an epoxy resin and inorganic filler and a mixture of an epoxy resin and inorganic filler. By doing so, it is possible to adjust the coefficients of thermal expansion between the resin filler and the core substrate.

20

Brief Description of Drawings

Fig. 1 is a diagram showing a process for manufacturing a multi-layer printed circuit board according to the first embodiment of the present invention;

25 Fig. 2 is a diagram showing a process for manufacturing the multi-layer printed circuit board according to the first embodiment;

Fig. 3 is a diagram showing a process for manufacturing the multi-layer printed circuit board according to the first embodiment;

5 Fig. 4 is a diagram showing a process for manufacturing the multi-layer printed circuit board according to the first embodiment;

Fig. 5 is a diagram showing a process for manufacturing the multi-layer printed circuit board according to the first embodiment;

10 Fig. 6 is a cross-sectional view of the multi-layer printed circuit board according to the first embodiment;

Fig. 7 is a table showing the evaluation results of the first embodiment and Comparison;

15 Fig. 8 is a diagram showing a process for manufacturing a multi-layer printed circuit board according to the second embodiment of the present invention;

Fig. 9 is a diagram showing a process for manufacturing the multi-layer printed circuit board according to the second embodiment;

20 Fig. 10 is a diagram showing a process for manufacturing the multi-layer printed circuit board according to the second embodiment;

Fig. 11 is a diagram showing a process for manufacturing the multi-layer printed circuit board according to the second embodiment;

25 Fig. 12 is a diagram showing a process for manufacturing the multi-layer printed circuit board according to the second

embodiment;

Fig. 13 is a cross-sectional view of the printed circuit board according to the second embodiment;

5 Fig. 14 is a diagram showing a process for manufacturing a multi-layer printed circuit board according to the first modification of the second embodiment;

Fig. 15 is a diagram showing a process for manufacturing the multi-layer printed circuit board according to the first modification of the second embodiment;

10 Fig. 16 is a diagram showing a process for manufacturing the multi-layer printed circuit board according to the first modification of the second embodiment;

Fig. 17 is a diagram showing a process for manufacturing the multi-layer printed circuit board according to the first modification of the second embodiment;

15 Fig. 18 is a diagram showing a process for manufacturing the multi-layer printed circuit board according to the first modification of the second embodiment;

Fig. 19 is a cross-sectional view of the multi-layer printed circuit board according to the first modification of the second embodiment;

Fig. 20 is a cross-sectional view of the multi-layer printed circuit board according to the second modification of the second embodiment;

25 Fig. 21 is a table showing the estimation result of the embodiments of the present invention and Comparisons; and

Fig. 22 is a cross-sectional view of a conventional

multi-layer printed circuit board.

Best Mode for Carrying Out the Invention

[First Embodiment]

5 The embodiments of the present invention will be described hereinafter with reference to the accompanying drawings.

First, the constitution of a multi-layer printed circuit board according to the first embodiment of the present invention will be described with reference to Fig. 6 showing a longitudinal 10 sectional view.

As shown in Fig. 6, a multi-layer printed circuit board 10 has a core substrate 30 having right and reverse sides on which buildup wiring layers 80U and 80D are formed, respectively. Each of the buildup wiring layers 80U and 80D consists of a lower 15 interlayer resin insulating layer 50 in which via holes 46 are formed, an upper interlayer resin insulating layer 60 in which upper via holes 66 are formed, and a solder resist layer 70 formed on the upper interlayer resin insulating layer 60. A solder bump (external connection terminal) 76 for connecting the board 20 10 to an IC chip (not shown) is formed on each of the upper via holes 66 through the opening portion 71 of the solder resist 70. A conductive connection pin (external connection terminal) 78 for connecting the circuit board 10 to a daughter board (not shown) is connected to each of the lower via holes 66.

25 In the first embodiment, through holes 36 connecting the buildup wiring layers 80U and 80D to each other are formed to penetrate a core substrate 30 and the lower interlayer resin

insulating layers 50. Resin filler 54 is filled in the through holes 36 and plated covers 58 are provided onto the opening portions of the holes 36. Likewise, resin filler 54 is filled in the via holes 46 formed in the lower interlayer resin insulating 5 layer 50 and plated covers 58 are provided onto the opening portions of the via holes 46.

In the first embodiment, the through holes 36 are formed to penetrate the core substrate 30 and the lower interlayer resin insulating layers 50 and the via holes 66 are formed right on the through holes 36, respectively. Due to this, each through hole 36 and each via hole 66 are arranged linearly to thereby make it possible to shorten wiring length and to accelerate signal transmission speed. Further, since the through holes 36 are directly connected to the via holes 66 connected to the external connection terminals (solder bumps 76, conductive connection pins 78), excellent connection reliability is obtained. In the first embodiment, as will be described later, the filler 54 filled in the through holes 36 is flattened by polishing and then the plated covers (conductive layers) 58 covering the filler 54 are arranged and the via holes 66 are formed thereon. Due to this, the surfaces of the through holes 36 have high flatness and reliability in the connection between the through holes 36 and the corresponding via holes 66 is excellent.

Furthermore, in case of the multi-layer printed circuit board in the first embodiment, the through holes 36 and the lower via holes 46 are filled with the same resin filler 54 and the resin filler 54 is simultaneously polished and flattened as will

be described later. Thus, the multi-layer printed circuit board can be manufactured at low cost and the strength of the interiors of the through holes and that of the interiors of the via holes can be kept uniform, so that the reliability of the multi-layer printed circuit board can be enhanced. Also, as will be described later, the filler 54 filled in the via holes 47 is flattened by polishing and then the plated covers (conductive layers) 58 covering the filler 54 are arranged and the upper via holes 66 are formed thereon. Due to this, the surfaces of the lower via holes 46 have high flatness and reliability in the connection between the lower via holes 46 and the upper via holes 66 is excellent.

Moreover, as will be described later, in case of the multi-layer printed circuit board in the first embodiment, a de-smear process for penetrating holes 35 which become the through holes 36 and a roughing process for the surface of the lower interlayer resin insulating layer 40 are performed simultaneously using an oxidizer, so that the number of manufacturing steps can be reduced and the multi-layer printed circuit board can be manufactured at low cost.

Next, description will be given to a method of manufacturing the multi-layer printed circuit board with reference to Figs. 1 to 5.

(1) A copper-clad laminated plate 30A having copper foils 32 each having a thickness of 18 μm and laminated on both sides of a substrate 30 having a thickness of 0.8 mm and made of a glass epoxy resin, FR4, FR5 or BT (Bismaleimide-Triazine) resin,

is employed as a starting material (Fig. 1(A)). First, this copper-clad laminated plate is etched in a pattern fashion, thereby forming inner-layer copper patterns 34 on the both sides of the substrate (Fig. 1(B)).

5 (2) After washing the substrate 30 on which the inner-layer copper patterns 34 are formed, an etching solution containing a cupric complex and an organic acid is reacted under oxygen coexisting conditions such as spraying or bubbling. The copper conductor of a conductor circuit is dissolved to form voids.

10 Through these processes, a rough layer 38 is provided on the surface of each inner-layer copper pattern 34 (Fig. 1(c)).

Alternatively, the rough layer may be provided by an oxidization-reduction process or by employing an electroless plated alloy. The rough layer thus formed has desirably a thickness in a range of 0.1 to 5 μm . In such a range, the separation between the conductor circuit and the interlayer resin insulating layer less occurs.

The cupric complex is preferably a cupric complex of azoles. The cupric complex of azoles functions as an oxidizer for oxidizing metallic copper or the like. Azoles preferably involve diazole, triazole and tetrazole. Particularly, imidazole, 2-methylimidazole, 2-ethylimidazole, 2-ethyl-4-methylimidazole, 2-phenylimidazole, 2-undecylimidazole and the like are preferable. The quantity of added cupric complex of azoles is preferably 1 to 15 wt%. This is because the cupric complex of such a quantity is excellent in solubility and stability.

Further, to dissolve the copper oxide, an organic acid is mixed with the cupric complex of azoles. To be specific, the organic acid is preferably at least one selected from a group consisting of formic acid, acetic acid, propionic acid, butyric acid, valeric acid, caproic acid, acrylic acid, crotonic acid, 5 oxalic acid, malonic acid, succinic acid, glutaric acid, maleic acid, benzoic acid, glycolic acid, lactic acid, malic acid and sulfamic acid. An organic acid content is preferably 0.1 to 30 wt%. With this content, it is possible to maintain the 10 solubility of the oxidized copper and to secure stable solubility.

The generated cuprous complex is dissolved by the acid, combined with oxygen into a cupric complex which contributes again to the oxidization of copper.

15 Furthermore, to assist in dissolving copper and oxidizing
azoles, halogen ions, such as fluorine ions, chlorine ions and
bromine ions, may be added to the etching solution. The present
invention can supply halogen ions by adding hydrochloric acid,
sodium chloride or the like. The quantity of halogen ions is
20 preferably 0.01 to 20 wt%. Halogen ions of such a quantity
ensures excellent adhesiveness between the generated rough
surface and the interlayer resin insulating layer.

The cupric complex of azoles and the organic acid (or halogen ions according to necessity) are dissolved in water to thereby adjust the etching solution. Further, a commercially available etching solution, e.g., product name "MEC etch BOND" manufactured by Mec Co., Ltd., can be employed to form a rough

surface according to the present invention.

(3) A resin film 50 α which becomes a lower interlayer resin insulating layer is bonded on each surface of the substrate 30 by vacuum crimp lamination at a pressure of 5kgf/cm² while raising 5 temperature to 50 to 150°C (Fig. 1(D)).

The resin film contains refractory resin, soluble particles, a curing agent and other components. The materials will now be described.

The resin film for use in the resin insulating layer in 10 the manufacturing method according to the present invention has a structure that particles soluble in acid or an oxidizer (hereinafter called "soluble particles") are dispersed in resin which is refractory with respect to acid or an oxidizer (hereinafter called "refractory resin").

15 The expressions "refractory" and "soluble" will now be described. When materials are immersed in solution composed of the same acid or the same oxidizers for the same time, a material of a type which is dissolved at a relatively high dissolving rate is called a "soluble" material for convenience. A material 20 of a type which is dissolved at a relatively slow dissolving rate is called a "refractory material" for convenience.

The soluble particles are exemplified by resin particles which are soluble in acid or an oxidizer (hereinafter called "soluble resin particles"), inorganic particles which are 25 soluble in acid or an oxidizer (hereinafter called "inorganic soluble particles") and metal particles which are soluble in acid or an oxidizer (hereinafter called "soluble metal

particles"). The foregoing soluble particles may be employed solely or two or more particles may be employed.

The shape of each of the soluble particles is not limited. The shape may be a spherical shape or a pulverized shape. It 5 is preferable that the particles have a uniform shape. The reason for this lies in that a rough surface having uniformly rough pits and projections can be formed.

It is preferable that the mean particle size of the soluble particles is $0.1\mu\text{m}$ to $10\mu\text{m}$. When the particles have the 10 diameters satisfying the foregoing range, particles having two or more particle sizes may be employed. That is, soluble particles having a mean particle size of $0.1\mu\text{m}$ to $0.5\mu\text{m}$ and soluble particles having a mean particle size of $1\mu\text{m}$ to $3\mu\text{m}$ may be mixed. Thus, a more complicated rough surface can 15 be formed. Moreover, the adhesiveness with the conductor circuit can be improved. In the present invention, the particle size of the soluble particles is the length of a longest portion of each of the soluble particles.

The soluble resin particles may be particles constituted 20 by thermosetting resin or thermoplastic resin. When the particles are immersed in solution composed of acid or an oxidizer, the particles must exhibit dissolving rate higher than that of the foregoing refractory resin.

Specifically, the soluble resin particles are exemplified 25 by particles constituted by epoxy resin, phenol resin, polyimide resin, polyphenylene resin, polyolefin resin or fluorine resin. The foregoing material may be employed solely or two or more

materials may be mixed.

The soluble resin particles may be resin particles constituted by rubber. Rubber above is exemplified by polybutadiene rubber, a variety of denatured polybutadiene 5 rubber, such as denatured epoxy rubber, denatured urethane rubber or denatured (metha) acrylonitrile rubber, and (metha) acrylonitrile butadiene rubber containing a carboxylic group. When the foregoing rubber material is employed, the soluble resin particles can easily be dissolved in acid or an oxidizer. That 10 is, when the soluble resin particles are dissolved with acid, dissolution is permitted with acid except for strong acid. When the soluble resin particles are dissolved, dissolution is permitted with permanganate which has a relatively weak oxidizing power. When chromic acid is employed, dissolution is permitted 15 even at a low concentration. Therefore, retention of the acid or the oxidizer on the surface of the resin can be prevented. When a catalyst, such as palladium chloride, is supplied after the rough surface has been formed as described later, inhibition of supply of the catalyst and oxidation of the catalyst can be 20 prevented.

The inorganic soluble particles are exemplified by particles made of at least a material selected from a group consisting of an aluminum compound, a calcium compound, a potassium compound, a magnesium compound and a silicon compound.

25 The aluminum compound is exemplified by alumina and aluminum hydroxide. The calcium compound is exemplified by calcium carbonate and calcium hydroxide. The potassium

compound is exemplified by potassium carbonate. The magnesium compound is exemplified by magnesia, dolomite and basic magnesium carbonate. The silicon compound is exemplified by silica and zeolite. The foregoing material may be employed solely or two or more materials may be mixed.

5 The soluble metal particles are exemplified by particles constituted by at least one material selected from a group consisting of copper, nickel, iron, zinc, lead, gold, silver, aluminum, magnesium, potassium and silicon. The soluble metal 10 particles may have surfaces coated with resin or the like in order to maintain an insulating characteristic.

When two or more types of the soluble particles are mixed, it is preferable that the combination of the two types of soluble 15 particles is combination of resin particles and inorganic particles. Since each of the particles has low conductivity, an insulating characteristic with the resin film can be maintained. Moreover, the thermal expansion can easily be adjusted with the refractory resin. Thus, occurrence of a crack of the interlayer resin insulating layer constituted by the resin 20 film can be prevented. Thus, separation between the interlayer resin insulating layer and the conductor circuit can be prevented.

The refractory resin is not limited when the resin is able to maintain the shape of the rough surface when the rough surface 25 is formed on the interlayer resin insulating layer by using acid or oxidizer. The refractory resin is exemplified by thermosetting resin, thermoplastic resin and their composite

material. As an alternative to this, the foregoing photosensitive resin of a type having photosensitive characteristic imparted thereto may be employed. When the photosensitive resin is employed, exposure and development processes of the interlayer resin insulating layers can be performed to form the openings for the via holes.

In particular, it is preferable that the resin containing thermosetting resin is employed. In the foregoing case, the shape of the rough surface can be maintained against plating solution and when a variety of heating processes are performed.

The refractory resin is exemplified by epoxy resin, phenol resin, phenoxy resin, polyimide resin, polyphenylene resin, polyolefin resin and fluorine resin. The foregoing material may be employed solely or two or more types of the materials may be mixed.

It is preferable that epoxy resin having two or more epoxy groups in one molecule thereof is employed. The reason for this lies in that the foregoing rough surface can be formed. Moreover, excellent heat resistance and the like can be obtained. Thus, concentration of stress onto the metal layer can be prevented even under a heat cycle condition. Thus, occurrence of separation of the metal layer can be prevented.

The epoxy resin is exemplified by cresol novolac epoxy resin, bisphenol-A epoxy resin, bisphenol-F epoxy resin, phenol novolac epoxy resin, alkylphenol novolac epoxy resin, biphenol-F epoxy resin, naphthalene epoxy resin, dicyclopentadiene epoxy resin, an epoxy material constituted by a condensation material

of phenol and an aromatic aldehyde having a phenol hydroxyl group, triglycidyl isocyanurate and alicyclic epoxy resin. The foregoing material may be employed solely or two or more material may be mixed. Thus, excellent heat resistance can be realized.

5 It is preferable that the soluble particles in the resin film according to the present invention are substantially uniformly dispersed in the refractory resin. The reason for this lies in that a rough surface having uniform pits and projections can be formed. When via holes and through holes 10 are formed in the resin film, adhesiveness with the metal layer of the conductor circuit can be maintained. As an alternative to this, a resin film containing soluble particles in only the surface on which the rough surface is formed may be employed. Thus, the portions of the resin film except for the surface is 15 not exposed to acid or the oxidizer. Therefore, the insulating characteristic between conductor circuits through the interlayer resin insulating layer can reliably be maintained.

It is preferable that the amount of the soluble particles which are dispersed in the refractory resin is 3 wt% to 40 wt% 20 with respect to the resin film. When the amount of mixture of the soluble particles is lower than 3 wt%, the rough surface having required pits and projections cannot be formed. When the amount is higher than 40 wt%, deep portions of the resin film are undesirably dissolved when the soluble particles are 25 dissolved by using acid or the oxidizer. Thus, the insulating characteristic between the conductor circuits through the interlayer resin insulating layer constituted by the resin film

cannot be maintained. Thus, short circuit is sometimes caused to occur.

It is preferable that the resin film contains a curing agent and other components as well as the refractory resin.

5 The curing agent is exemplified by an imidazole curing agent, an amine curing agent, a guanidine curing agent, an epoxy adduct of each of the foregoing curing agents, a microcapsule of each of the foregoing curing agents and an organic phosphine compound, such as triphenylphosphine or tetraphenyl phosphonium 10 tetraphenyl borate.

It is preferable that the content of the curing agent is 0.05 wt% to 10 wt% with respect to the resin film. When the content is lower than 0.05 wt%, the resin film cannot sufficiently be hardened. Thus, introduction of acid and the oxidizer into 15 the resin film occurs greatly. In the foregoing case, the insulating characteristic of the resin film sometimes deteriorates. When the content is higher than 10 wt%, an excessively large quantity of the curing agent component sometimes denatures the composition of the resin. In the 20 foregoing case, the reliability sometimes deteriorates.

The other components are exemplified by an inorganic compound which does not exert an influence on the formation of the rough surface and a filler constituted by resin. The inorganic compound is exemplified by silica, alumina and dolomite. 25 The resin is exemplified by polyimide resin, polyacrylic resin, polyamideimide resin, polyphenylene resin, melanine resin and olefin resin. When any one of the foregoing fillers is contained,

conformity of the thermal expansion coefficients can be established. Moreover, heat resistance and chemical resistance can be improved. As a result, the performance of the printed circuit board can be improved.

5 The resin film may contain solvent. The solvent is exemplified by ketone, such as acetone, methylethylketone or cyclohexane; aromatic hydrocarbon, such as ethyl acetate, butyl acetate, cellosolve acetate, toluene or xylene. The foregoing material may be employed solely or two or more materials may
10 be mixed.

(4) Next, penetrating holes 35 each having a diameter of 300 μm are formed in the core substrate 30 to which the resin films 50 α have been bonded, for forming through holes (Fig. 1(E)).

(5) Via hole openings 52 each having a diameter of 80 μm are formed in the resin films 50 α by applying carbonic acid, excimer, YAG or UV laser (Fig. 2(A)). Thereafter, the resin films 50 α are thermally hardened to thereby form lower interlayer resin insulating layers 50. The via holes may be formed by an area process using laser or an area process using laser with masks mounted. Alternatively, mixture laser (which means a mixture of, for example, carbonic acid laser and excimer laser) may be employed. Alternatively, both the through holes and the via holes may be formed by using laser.

(6) Next, an oxidizer consisting of a chromic acid or a permanganate (e.g., potassium permanganate or sodium permanganate) is used to subject the penetrating holes 35 for forming through holes formed in the core substrate 30 and the

lower interlayer resin insulating layers 50 to a de-smear process and, at the same time, the surfaces of the lower interlayer resin insulating layers 50 are roughened (Fig. 2(B)). While temperature for performing these processes is set at 65°C herein, 5 the processes may be performed at temperature which fall within a range of 40 to 70°C.

The rough surfaces of the interlayer resin insulating layers are formed to have a thickness in a range of 0.5 to 5 mm. The thickness in that range can ensure adhesiveness and 10 the interlayer resin insulating layers can be removed in a later step.

The multi-layer printed circuit board in the first embodiment has the core substrate 30 consisting of one of an FR4 resin, an FR5 resin or a BT resin and has the lower interlayer 15 resin insulating layers 50 containing at least one of an epoxy resin, a phenol resin, a polyimide resin, a polyphenylene resin, a polyolefin resin, a fluorocarbon resin. It is, therefore, possible to simultaneously perform the de-smear process using an oxidizer consisting of a chromic acid and a permanganate to 20 the through holes 35 and the roughing process to the lower interlayer resin insulating layers 50. Thus, the number of steps is reduced to thereby manufacture the multi-layer printed circuit board at low cost. An electroless plated film is formed to have a thickness in a range of 0.1 to 5 μm . If having a thickness 25 in that range, the electroless plated film can be formed entirely and easily etched away.

(7) A palladium catalyst is applied to the roughed surfaces

of the interlayer resin insulating layers 50 to form electroless copper plated films 42 in an electroless plating solution (Fig. 2(C)). While the electroless copper plated films are formed herein, copper or nickel coats may be formed by sputtering.

5 Alternatively, the surface layers may be subjected to a plasma, UV or corona process as a drying process. Through the process, the surfaces of the layers 50 are reformed.

(8) After washing the substrate on which the electroless copper plated films 42 have been formed, plating resists 43 each having 10 a predetermined pattern are formed (Fig. 2(D)).

(9) The substrate is immersed in an electroplating solution to supply an electric current thereto through the electroless copper plated films 42, thereby forming electroplated copper films 44 (Fig. 2(E)).

15 (10) The plating resists 43 are separated and removed with KOH and the electroless copper plated films 42 under the plating resists are etched away by light etching, thereby forming via holes 46 and through holes 36 each consisting of the electroless copper plated film 42 and the electroplated copper film 44 (Fig. 20 3(A)).

(11) A rough layer (made of an alloy consisting of Cu-Ni-P) 47 is formed in each of the via holes 46 and the through holes 36 by electroless plating (Fig. 3(B)). Instead of electroless copper plating, the rough layer can be formed by etching (e.g., 25 etching by spraying or immersing the holes by or into a solution of a mixture of a cupric complex and an organic acid salt) or by an oxidization-reduction process.

(12) Resin filler 54 is prepared to have a viscosity of 50Pa·S at 23°C, masks having openings according to the diameters of the through holes 36 and the via holes 46, respectively, are mounted, the resin filler 54 is filled by printing and dried 5 in a drying furnace at a temperature of 100°C for 20 minutes (Fig. 3(C)). In the first embodiment, the same filler is simultaneously filled in the through holes 36 and the via holes 46, so that the number of manufacturing steps can be reduced.

Here, as the resin filler, the following material 10 compositions can be employed:

[Resin Composition]

100 parts by weight of bisphenol F epoxy monomer (YL983U having a molecular weight of 310 and manufactured by Yuka Shell), 72 parts by weight of SiO₂ spherical particles having 15 a surface coated with a silane coupling agent and having a mean particle diameter of 1.6 μm (CRS 101-1-CE manufactured by Admatec, where the maximum particle size is not larger than the thickness (15 μm) of an inner-layer copper pattern to be described later), 6.5 parts by weight of an imidazole curing agent (2E4MZ-CN 20 manufactured by Shikoku Chemicals) and 1.5 parts by weight of a leveling agent (PERENOL S4 manufactured by SANNOPCO) are stirred and mixed to thereby adjust the viscosity of the resultant mixture to 36,000 to 49,000 cps at 23±1°C.

(13) One side of the substrate 30 for which the process of (12) 25 has been completed, is polished so as to flatten the surface of the resin filler 54 protruding from the openings of the via holes 46 and the through holes 36. Then, buffing is conducted

once or a plurality of times to remove flaws caused by polishing. The series of polishing processes are also conducted to the other side of the substrate (Fig. 3(D)).

It is noted that the protruded resin filler can be removed
5 and flattened only by buffing.

The advantage of conducting buffing is that various types of particles are contained in the interlayer resin insulating layers and are not scraped away during polishing.

Next, the resin filler 54 is hardened by conducting a heat
10 process at 100°C for one hour and at 150°C for one hour.

Thus, a resin filler layer having the hardened resin filler containing the epoxy resin, the curing agent and the inorganic particles, is formed in each through hole.

While the epoxy resin is not limited to a particular resin,
15 it is preferably at least one selected from a group consisting of bisphenol epoxy resins and novolac resins. This is because if a bisphenol A or F epoxy resin is selected, the viscosity of the resultant mixture can be adjusted without using a dilution solvent. In addition, novolac epoxy resins are excellent in
20 strength, heat resistance and chemical resistance, are not decomposed even in a strong base solution such as electroless plating solution and are not thermally decomposed.

As the bisphenol epoxy resin, a bisphenol A epoxy resin or a bisphenol F epoxy resin is preferable. The bisphenol F epoxy resin is more preferable because it can be employed with a low viscosity and without using a solvent.

Further, as the novolac epoxy resin, at least one selected

from phenol novolac epoxy resins and cresol novolac epoxy resins is preferable.

Alternatively, a mixture of a bisphenol epoxy resin and a novolac epoxy resin may be employed.

5 In the latter case, a mixture ratio of, for example, the bisphenol epoxy resin to the cresol novolac epoxy resin is preferably 1/1 to 1/100. By mixing the bisphenol epoxy resin and the cresol novolac epoxy resin with each other in that range, it is possible to suppress the viscosity of the resultant mixture
10 from rising.

The curing agent contained in the resin filler is not limited to a particular one and a well-known curing agent is available; however, an imidazole curing agent or an amine curing agent is preferable. If such a curing agent is employed, the
15 contraction degree of the filler when the filler is hardened is small and the adhesiveness between the conductor layer constituting the through holes and the resin filler layer is particularly excellent.

Further, the inorganic particles contained in the resin
20 filler may consist of, for example, aluminum compounds, calcium compounds, potassium compounds, magnesium compounds, silicon compounds and the like. They may be used solely or two or more of them may be employed.

The aluminum compounds involve, for example, alumina, aluminum hydroxide and the like. The calcium compounds involve, for example, calcium carbonate, calcium hydroxide and the like. The magnesium compounds involve, for example, magnesia, dolomite,

basic magnesium carbonate, talc and the like. The silicon compounds involve, for example, silica, zeolite and the like.

The resin filler contains inorganic particles of 10 to 50 wt%. The inorganic particle content in that range allows 5 matching thermal expansion coefficients between the interlayer resin insulating layers. It is more preferable that the resin filler contains inorganic particles of 20 to 40wt%.

The shapes of the inorganic particles involve spherical, circular, ellipsoidal, pulverized, polygonal shapes. Among 10 them, the spherical, circular and ellipsoidal shapes are more preferable. This is because these shapes can suppress the occurrence of cracks and the like resulting from particle shapes. Further, the particles may be coated with a silica coupling agent. By doing so, the adhesiveness between the inorganic particles 15 and the epoxy resin improves.

It is also preferable that a rough surface is formed on at least part of the surface of the conductor layers constituting the through holes. If so, the adhesiveness between the conductor layers and the resin filler layers further improves and expansion 20 and contraction in a heat history can be suppressed to thereby make it more difficult to separate the conductor layers from the resin filler layers. The mean roughness of the rough surface is preferably 0.05 to 5 μm . If the mean roughness is less than 0.05 μm , the effect of roughing the surfaces of the conductor 25 layers is hardly obtained. If the mean roughness exceeds 5 μm , signal delays and signal errors resulting from a skin effect at the time of signal transmission may possibly occur.

The resin filler may contain not only the epoxy resin but also other thermosetting resins, thermoplastic resins, photosensitive resins, complexes thereof or the like.

The thermosetting resins involve, for example, a polyimide resin and a phenol resin. The thermoplastic resins involve, for example, a fluorocarbon resin such as polytetrafluoroethylene (PTFE), tetrafluoroethylene/hexafluoropropylene copolymer (fluorinated ethylene propylene) (FEP) and 10 tetrafluoroethylene/perphloroalkoxy copolymer (PFA), polyethylene terephthalate (PET), polysulfone (PSF), polyphenylene sulfide (PPS), thermoplastic polyphenylene ether (PPE), polyether sulfone (PES), polyetherimide (PEI), polyphenylene sulfone (PPES), polyethylene naphthalate (PEN), 15 poly(ether ether ketone) (PEEK), polyolefin and phenoxy resins.

The photosensitive resins involve, for example, acrylic resins by adding a (meta) acrylic acid having photosensitive groups to part of thermosetting resins. These resins may be used solely or two or more resins may be employed. Instead of the epoxy resin, these resins or complexes thereof (i.e., a complex of a thermosetting resin and a thermoplastic resin or a complex of a photosensitive resin and a thermoplastic resin) may be employed.

Further, resin particles, metallic particles and the like other than the inorganic particles may be mixed with the resin filler. The resin particles involve those obtained by spherizing thermosetting resins, thermoplastic resins and the like. The

metallic particles involve conductive particles such as gold, silver and copper particles and the like. They may be used solely or two types or more particles may be employed. Alternatively, they may be employed instead of the inorganic particles.

5 The resin filler may contain a solvent such as NMP (N-methylpyrrolidone), DMDG (diethylene glycol dimethyl ether), glycerol, cyclohexanol, cyclohexanone, methyl cellosolve, methyl cellosolve acetate, methanol, ethanol, butanol or propanol, (solvent-impregnated type); however, it is more
10 preferable that the resin filler contains no solvent (non-solvent-containing type). This is because air bubble is less left in the through holes and the like after hardening the resin filler if the resin filler contains no solvent. If air bubble is left, reliability and connection characteristics
15 deteriorate.

(14) A palladium catalyst is applied to the surfaces of the interlayer resin insulating layers 50 to thereby form electroless copper plated films 56 in an electroless plating solution (Fig. 4(A)). While the electroless copper plated films are formed
20 herein, copper or nickel coats can be formed by sputtering. In some cases, electroplating can be directly performed to the interlayer resin insulating layers 50.

(15) After forming plating resists (not shown) each having a predetermined pattern, electroplated copper films 57 are formed.
25 Then, the plating resists are separated and removed and the electroless copper plated films 56 under the plating resist are separated by light etching, thereby forming plated covers 58

each consisting of the electroless copper plated film 56 and the electroplated copper film 57 in the opening portions of the via holes 46 and the through holes 36, respectively (Fig. 4(B)).

(16) Rough layers (Cu-Ni-P) are formed on the plated covers 5 58 provided on the openings of the via holes 46 and the through holes 36 by electroless plating, respectively (Fig. 4(C)). The rough layers can be formed by etching or an oxidization-reduction process instead of the electroless copper plating.

(17) By repeating the steps (3) to (11) described above, upper 10 interlayer resin insulating layers 60 are formed and via holes 66 each consisting of the electroless copper plated film 62 and the electroplated copper film 64 on the upper interlayer resin insulating layers 60 (Fig. 4(D)).

(18) Next, solder resists and solder bumps are formed. The 15 material composition of the solder resist is as follows.

46.67 g of oligomer (having a molecular weight of 4000) which is obtained by forming 50% of epoxy groups of 60 wt% cresol novolac epoxy resin (manufactured by Nippon Kayaku) dissolved in DMDG into an acrylic structure and which imparts 20 photosensitive characteristic, 15.0 g of 80 wt% bisphenol A epoxy resin (Epicoat 1001 manufactured by Yuka Shell) dissolved in methyl ketone, 1.6 g of an imidazole curing agent (2E4MZ-CN manufactured by Shikoku Chemicals), 3 g of polyhydric acrylic monomer which is photosensitive monomer (R604 manufactured by Nippon Kayaku), 1.5 g of polyhydric acrylic monomer (DPE6A manufactured by Kyoei Chemical) and 0.71 g of a dispersing deforming agent (S-65 manufactured by SANNOPCO) are mixed with

one another. Then, 2 g of benzophenone (manufactured by Kanto Chemical) serving as a photoinitiator and 0.2 g of Michler's ketone (manufactured by Kanto Chemical) serving as a photosensitizer are added to the resultant mixture, thereby 5 obtaining a solder resist composition having a viscosity adjusted to 2.0 Pa·s at 25°C.

For the solder resist layers, various types of resins may be used. For example, a resin obtained by hardening a bisphenol A epoxy resin, a bisphenol A epoxy acrylate resin, a novolac 10 epoxy resin or a novolac epoxy acrylate resin by an amine curing agent, an imidazole curing agent or the like can be used.

In case of forming a solder bump by providing an opening in the solder resist layer, in particular, it is preferable to use a resin containing "a novolac epoxy resin or a novolac epoxy 15 acrylate resin" and containing "an imidazole curing agent" as a curing agent.

The above solder resist composition 70a is applied to each side of the multi-layer printed circuit board obtained in the step (17) to have a thickness of 40 µm (Fig. 5(A)).

20 (19) Then, a drying process is performed at 70°C for 20 minutes and at 80°C for 30 minutes. Thereafter, a photomask film which has a thickness of 5 mm and on which a circular pattern (mask pattern) drawn is made hermetic contact with the both sides of the resultant multi-layer printed circuit board, mounted thereon, 25 exposed with ultraviolet rays with 1000 mJ/cm² and subjected to a DMTG development process. Further, a heat process is performed on conditions of 80°C for one hour, 100°C for one hour,

120°C for one hour and 150°C for three hours, to thereby form solder resist layers 70 (a thickness of 20 μm) each having opening portions 71 (an opening diameter of 200 μm) (Fig. 5(B)).

(20) Thereafter, the multi-layer printed circuit board is 5 immersed in an electroless nickel plating solution composed of 2.3×10^{-1} mol/l sodium hypophosphite and 1.6×10^{-1} mol/l sodium citrate and having pH = 4.5 for 20 minutes. Thus, a nickel plated layer 72 having a thickness of 5 μm is formed in each opening portion 71. Then, the multi-layer printed circuit board is 10 immersed in an electroless gold plating solution composed of 7.6×10^{-3} mol/l gold potassium cyanide, 1.9×10^{-1} mol/l ammonia chloride, 1.2×10^{-1} mol/l sodium citrate and 1.7×10^{-1} mol/l sodium hypophosphite on conditions of 80°C for 7.5 minutes. Thus, gold plated layers 74 each having a thickness of 0.03 μm are formed 15 on the nickel plated layers 72, respectively (Fig. 5(C)).

In the above-stated case, the intermediate layer is formed out of nickel and the noble metal layer out of gold.

Alternatively, the intermediate layer may be formed out of palladium, tin or titanium instead of nickel and the noble metal 20 layer may be formed out of silver, platinum or the like other than gold. Two or more noble metal layers may be formed. As surface processes, a drying process, a plasma process, a UV process and a corona process may be performed. By doing so, it is possible to enhance the filling efficiency of the 25 under-filler for the IC chip.

(23) Then, a solder paste is printed on each opening 71 of the solder resist layer 70 and a reflow process is conducted to thereby

form a solder bump (solder) 76 in each of the upper surface-side via holes 66. Also, a conductive connection pin 78 is attached to each of the lower surface-side via holes 66 through the solder 77 (see Fig. 6). It is also possible to form a BGA instead of 5 the conductive connection pin.

As the solder, Sn/Pb, Sn/Sb, Sn/Ag, Sn/Sb/Pb, Sn/Ag/Cu and the like may be used.

The melting point of the solder is preferably 180 to 280°C. The solder having the melting point in that range can ensure 10 that the conductive connection pin has a strength of 2.0 Kg/pin or higher. If the melting point is lower than that range, the strength of the pin decreases. If exceeding the range, the solder resist layer may possibly be dissolved. It is particularly preferable that the melting point of the solder is 200 to 260°C.

15 It is more preferable that the melting point of the solder at the conductive connection pin side is higher than that of the solder at the solder bump side. By doing so, conductive connection pins are not inclined or detached during reflow if an IC chip is mounted as a flip chip. A combination of solders 20 is, for example, Sn/Pb at the solder bump side and Sn/Sb at the conductive connection pin side.

[Comparison Example 1]

As a comparison example 1, a multi-layer printed circuit 25 board was obtained which board is the same in constitution as the multi-layer printed circuit board in the first embodiment shown in Fig. 1 and which has lower via holes filled with copper

plated layer. The evaluation results of the multi-layer printed circuit board in the first embodiment and that in the comparison example 1 are shown in Fig. 7.

Electrical connection characteristic was evaluated by 5 inspecting continuity using a checker. If short circuit and disconnection occurred, the multi-layer printed circuit board was judged NG and otherwise, judged OK. The separation and expansion thereof were inspected by cutting the multi-layer printed circuit boards in cross section after a heat cycle test 10 (in which 1000 cycles were repeated with one cycle set as -65°C / 3 minutes + 130°C / 3 minutes) and then visually inspecting the separation and expansion of the interlayer resin insulating layers and the via holes using a microscope (×100 to 400).

In the comparison example 1, dents which were not 15 completely filled with a plated material were formed on the surfaces of the lower via holes and the connection characteristic between the upper and lower via holes deteriorated. Due to this, there were some via holes which were not electrically connected to each other.

Further, after the heat cycle test, it was observed that 20 because of the separation between the via holes, the separation and expansion occurred to the interlayer resin insulating layers. In the multi-layer printed circuit board in the first embodiment, the connection characteristics did not deteriorate and the 25 separation and expansion were not observed.

[Comparison Example 2]

As a comparison example 2, a multi-layer printed circuit board was obtained which board is the same in constitution as the multi-layer printed circuit board in the first embodiment shown in Fig. 6 and which has the resin filler used in the first embodiment and filled in through holes and has a metal paste mainly consisting of a silver paste and filled in via holes. 5 In the multi-layer printed circuit board in the comparison example 2, the coefficient of the thermal expansion of the via holes 66 filled with the metal paste greatly differed from that 10 of the through holes 26 filled with the resin filler. Due to this, a force transferred to the lower interlayer resin insulating layers 50 from the lateral direction varies and the interlayer resin insulating layers 50 expanded or separated from a core substrate 30. In the embodiment stated above, by contrast, 15 the separation of the lower interlayer resin insulating layers 50 did not occur.

When a heat cycle test was conducted (in which 1000 cycles were repeated with one cycle set as -65°C / 3 minutes + 130°C / 3 minutes), the connection characteristics and adhesiveness 20 did not deteriorate in the embodiment. In the comparison example 2, because of the difference in filler material, it was observed that the adhesiveness of some parts deteriorated and the separation of the interlayer resin insulating layers occurred.

25 [Comparison Example 3]

A comparison example 3 is almost the same as the first embodiment except that the quantity of mixed silica was 271 parts

by weight and that the mixture ratio of inorganic particles to resin filler was 71.5 wt%.

[Comparison Example 4]

5 A comparison example 4 is almost the same as the first embodiment except that the quantity of mixed silica was 5.7 parts by weight and that the mixture ratio of inorganic particles to resin filler was 5.0 wt%.

10 In the comparison example 3, it was observed that cracks occurred to the resin filler under heat cycle conditions. In the comparison example 4, the surface portion of the resin filler was not polished flat and insufficiently polished portions and recessed portions resulting from the separation of inorganic particles were observed. Further, it was observed that the 15 thicknesses of the plated films on the resin filler were uneven or the plated films were not deposited.

[Second Embodiment]

20 The constitution of a printed circuit board according to the second embodiment of the present invention will be described hereinafter with reference to Fig. 13 which is a cross-sectional view of a printed circuit board 110.

25 The printed circuit board 110 consists of a core substrate 130 and buildup wiring layers 180A and 180B. Each of the buildup wiring layers 180A and 180B consists of interlayer resin insulating layers 150 and 160. Via holes 146 and conductor circuits 145 are formed on the interlayer resin insulating layers

150. Via holes 166 and conductor circuits 165 are formed on the interlayer resin insulating layers 160. Solder resist layers 170 are provided on the respective interlayer resin insulating layers 160.

5 Next, description will be given to a method of manufacturing the printed circuit board according to the second embodiment of the present invention. Here, A. interlayer resin insulating films used for manufacturing the printed circuit board in the second embodiment will be described, while B. resin filler 10 will not be described since the resin filler is the same in material composition as the resin filler used in the first embodiment.

A. Manufacture of a resin film for forming the interlayer resin insulating layers:

30 parts by weight of a bisphenol A epoxy resin (Epicoat 15 1001 having an epoxy equivalent of 469 and manufactured by Yuka Shell), 40 parts by weight of a cresol novolac epoxy resin (Epichron N-673 having an epoxy equivalent of 215 and manufactured by Dainippon Ink & Chemicals) and 30 parts by weight of a phenol novolac resin containing triazine structure 20 (Phenolight KA-7052 having a phenol hydroxyl group equivalent of 120 and manufactured by Dainippon Ink & Chemicals) were heated and dissolved in 20 parts by weight of ethyl diglycol acetate and 20 parts by weight of solvent naphtha while being stirred. Then, 15 parts by weight of polybutadiene rubber having epoxy 25 terminal (Denalex R-45EPT manufactured by Nagase Chemicals), 1.5 parts by weight of pulverized 2-phenyl-4, 5 bis(hydroxymethyl) imidazole, 2 parts by weight of particle-size

reduced silica and 0.5 parts by weight of a silicon defoaming agent were added thereto, thus preparing an epoxy resin composition. The obtained epoxy resin composition was applied onto a PET film having a thickness of 38 μm by using a roll coater 5 so that the thickness of the film was 50 μm after the film was dried, and dried at 80 to 120 $^{\circ}\text{C}$ for 10 minutes, thereby manufacturing the resin film for forming an interlayer resin insulating layer.

The description of the method of manufacturing the printed 10 circuit board stated above with reference to Fig. 13 will be continued with reference to Figs. 8 to 13.

(1) A copper-clad laminated plate 130A having copper foils 132 each having a thickness of 18 μm and laminated on the both sides of a substrate 130 having a thickness of 0.8 mm and made 15 of a glass epoxy resin or a BT (Bismaleimide-Triazine) resin is employed as a starting material (Fig. 8(A)). First, this copper-clad laminated plate 130A is drilled, subjected to an electroless plating process and etched in a pattern fashion, thereby forming lower conductor circuits 134 and through holes 20 136 on the both sides of the substrate 130 (Fig. 8(B)).

(2) After washing and drying the substrate 130 on which the through holes 136 and the lower conductor circuits 134 have been formed, a blackening process using a solution containing NaOH (10 g/l), NaClO₂ (40 g/l) and Na₃PO₄ (6 g/l) as a blackening bath 25 (oxidization bath) and a reduction process using a solution containing NaOH (10 g/l) and NaBH₄ (6 g/l) as a reduction bath are conducted to thereby form rough layers 134 α and 136 α on the

entire surfaces of the lower conductor circuits 134 including the through holes 136 (Fig. 8(C)). The roughing process may be surface roughing or the like by conducting soft etching, by forming a needle-type alloy plated material consisting of 5 copper-nickel-phosphorous (Interplate manufactured by EBARA UDYLITE Co., Ltd.) or by using an etching solution such as "MEC etch BOND" manufactured by Mec Co., Ltd.

(3) Next, the surfaces of the lands 136a of the through holes 136 having the rough layers 136 α formed thereon, respectively, 10 are polished by buffing and the rough layers 136 α of the lands 136a are separated to flatten the surfaces of the lands 136a (Fig. 8(D)).

(4) The resin filler described in B above is prepared, a mask 139 having opening portions 139a corresponding to the respective 15 through holes 36 is mounted on the substrate 130 within 24 hours of the preparation of the resin filler, and the resin filler 154 is pushed into the through holes 136 using a squeegee and dried on conditions of 100°C for 20 minutes (Fig. 9(A)). In the step of (3) above, after forming the rough layers 136 α on 20 the through holes 136, the surfaces of the lands 136a of the through holes 136 are polished and flattened. Due to this, when filling the resin filler in the through holes 136, it is possible to prevent the resin filler 154 from flowing out along the rough layers (anchors) formed on the lands 136a of the through holes 25 136. It is, therefore, possible to form the filler 154 in the through holes flat and to enhance the reliability of wirings above the through holes to be formed in a step described later.

Furthermore, the layers of resin filler 154 are formed on portions on which the lower conductor circuits 134 are not formed using a squeegee and dried on conditions of 100°C for 20 minutes (Fig. 9(B)). As the resin filler 154, it is preferable to employ one selected from a mixture of an epoxy resin and organic filler, a mixture of an epoxy resin and inorganic filler and a mixture of an epoxy resin and inorganic fiber. Alternatively, the resin filler in the first embodiment may be employed.

(5) One side of the substrate 130 for which the process described in (4) above has been completed, is polished by belt sander polishing using #600 belt abrasive paper (manufactured by Sankyo) in such a manner that the resin filler 154 is not left on the surfaces of the lower conductor circuits 134 and those of the lands 136a of the through holes 136. Then, buffing is performed to remove flaws caused by the belt sander polishing. These series of polishing are also conducted to the other side of the substrate 130 (Fig. 9(C)). Next, the resin filler 154 is hardened by performing a heating process at 100°C for one hour and 150°C for one hour.

Thus, the surface portion of the resin filler 154 filled between the lower conductor circuits 134 and in the through holes 136 and the rough surfaces 134a on the upper surfaces of the lower conductor circuits 134 are removed to thereby flatten the both sides of the substrate. By doing so, it is possible to obtain a wiring substrate in which the resin filler 154 and, the lower conductor circuits 134 and the through holes 136 are fixedly bonded through the rough layers 134a and 136a.

(6) After washing the substrate 130 and degreasing the substrate 130 with an acid, the substrate 130 is subjected to soft etching and an etching solution is sprayed on the both sides of the substrate 130 to etch the surfaces of the lower conductor circuits 134 and the surfaces of the lands 136a of the through holes 136, thereby forming rough surfaces 134β on the entire surfaces of the lands 136a of the through holes 136 and the lower conductor circuits 134 (Fig. 9(D)). As the etching solution, an etching solution containing 10 parts by weight of imidazole copper (II) complex, 7 parts by weight of a glycolic acid and 5 parts by weight of potassium chloride (MEC etch BOND manufactured by Mec Co., Ltd.) Each of the rough layers thus formed preferably has a thickness in a range of 0.1 to 5 μm . In that range, the separation between the conductor circuits and the interlayer resin insulating layers less occurs.

(7) Resin films for forming interlayer resin insulating layers slightly larger than the substrate 130 manufactured in A are mounted on the both sides of the substrate 130, temporarily pressed on conditions of a pressure of 4 kgf/cm², a temperature of 80°C and a press duration of 10 seconds and cut. Then, the resin films are bonded using a vacuum laminator device by the following method, thereby forming interlayer resin insulating layers 150 on the both sides of the substrate 130 (Fig. 10(A)). Namely, the resin films for forming the interlayer resin insulating layers are actually pressed on the both sides of the substrate on conditions of the degree of vacuum of 0.5 Torr, a pressure of 4 kgf/cm², a temperature of 80°C and a press duration

of 60 seconds and then thermally hardened at 170°C for 30 minutes.

(8) Next, via hole openings 152 each having a diameter of 80 μm are formed on the interlayer resin insulating layers 150 through masks 151 each having a thickness of 1.2 mm and having 5 penetrating holes 151a formed therein, by using CO₂ gas laser at a wavelength of 10.4 μm on conditions of a beam diameter of 4.0 mm, a top-hat mode, a pulse width of 8.0 microseconds, the diameter of each penetrating hole 151a of the masks 151 of 1.0 mm and one shot (Fig. 10(B)).

10 (9) The substrate 130 having the via hole openings 152 formed therein is immersed in a solution containing 60 g/l of a permanganate acid at a temperature of 80°C and epoxy resin particles existing on the surfaces of the interlayer resin insulating layers 150 are dissolved and removed, thereby forming 15 rough surfaces 150 α on the surfaces of the interlayer resin insulating layers 150 including the inner walls of the via hole openings 152 (Fig. 10(C)). The rough surfaces of the interlayer resin insulating layers are formed to have a thickness in a range of 0.5 to 5 μm . In that range, adhesiveness can be ensured and 20 the conductor layers can be removed in a later step.

(10) Next, the substrate 130, for which the above stated processes have been completed, is immersed in a neutral solution (manufactured by Siplay) and washed. A palladium catalyst is applied to the surfaces of the substrate 130 which surfaces have 25 been roughed (with a rough depth of 3 μm), thereby attaching catalyst cores on the surfaces of the interlayer resin insulating layers 150 and the inner wall surfaces of the via hole openings

152.

(11) Then, the substrate 130 is immersed in an electroless copper plating solution having the following composition to form electroless copper plated films 156 each having a thickness of 5 0.5 to 5.0 μm on the entire rough surfaces 150 α (Fig. 10(D)).

[Electroless Plating Solution]

NiSO ₄	0.003 mol/l
tartaric acid	0.200 mol/l
copper sulfate	0.030 mol/l
HCHO	0.050 mol/l
NaOH	0.100 mol/l
α,α -bipyridyl	40 mg/l
polyethylene glycol (PEG)	0.10 g/l

[Electroless Plating Conditions]

40 minutes at a solution temperature of 35°C.

10 (12) Commercially available photosensitive dry films are bonded onto the electroless copper plated films 156. Masks are mounted on the films, respectively and the films are exposed with 100 mj/cm^2 and developed with a 0.8% sodium carbonate solution, thereby providing plating resists 155 each having a 15 thickness of 30 μm . Then, the substrate 130 is washed with water of a temperature of 50°C and degreased, washed with water of a temperature of 25°C and with a sulfuric acid, and subjected to copper electroplating on the following conditions, thereby forming electroplated copper films 157 each having a thickness 20 of 20 μm (Fig. 11(A)).

[Electroplating Solution]

Sulfuric acid 2.24 mol/l

Copper sulfate 0.26 mol/l

Additive 19.5 mol/l

(Kaparacid HL manufactured by Atotech Japan)

[Electroplating Conditions]

Current density 1A/dm²

Duration 65 minutes

temperature 22±2°C

5

(13) After separating and removing the plating resists 155 with 5% NaOH, the electroless plated films 156 under the plating resists 155 are etched with a solution mixture of a sulfuric acid and hydrogen peroxide to remove and dissolve the films 156, thereby forming conductor circuits 145 (including via holes 146) each consisting of the electroless copper plated film 156 and the electroplated copper film 157 and having a thickness of 18 μ m (Fig. 11(B)).

10

(14) The same process as that in (6) is performed, i.e., rough surfaces 145 α are formed on the respective conductor circuits 145 by employing an etching solution containing a cupric complex and an organic acid (Fig. 11(C)).

15

(15) The steps of (7) to (14) are repeated, thereby forming interlayer resin insulating layers 160 and conductor circuits 165 (including via holes 166) further above (Fig. 11(D)).

20

(16) Next, a solder resist composition prepared in the same

manner as that in the first embodiment is obtained.

(17) The solder resist composition is applied to each side of the substrate 130 to have a thickness of 20 μm and dried. Then, a photomask is closely attached to each solder resist layer 170, 5 exposed to ultraviolet rays, developed with a DMTG solution to form openings 171U and 171D each having a diameter of 200 μm . Thereafter, a heating process is performed to harden the solder resist layers 170 to thereby provide the solder resist layers 170 each having openings 171U and 171D and each having a thickness 10 of 20 μm (Fig. 12(A)). The solder resist composition may be a commercially available solder resist composition.

(18) The substrate 130 having the solder resist layers 170 formed thereon is immersed in the same electroless nickel plating solution as that employed in the first embodiment and then 15 immersed in an electroless gold plating solution, thereby forming a nickel plated layer 172 and a gold plated layer 174 in each of the openings 171U and 171D (Fig. 12(B)).

(19) Thereafter, a solder paste containing tin-lead is printed on each opening 171U of the solder resist layers 170 of the 20 substrate 130. Further, a solder paste as a conductive adhesive agent 197 is printed on each opening 171 at the other side of the substrate. Next, conductive connection pins 178 are attached to and supported by an appropriate pin holding device and the fixed portions 198 of the respective conductive 25 connection pins 178 are brought into contact with the conductive adhesive agent 197 within the openings 171D. A reflow process is then performed to fix each conductive connection pin 178 to

the conductive adhesive agent 197. Alternatively, to attach the conductive connection pins 178, the conductive adhesive agent 197 may be formed into a ball shape or the like and put in the openings 171D, or the conductive adhesive agent 197 may be joined 5 to the fixed portions 198 to attach the conductive connection pins 178, followed by a reflow process. By doing so, it is possible to obtain a printed circuit board 110 having the solder bumps 176 and the conductive connection pins 178 (Fig. 13).

10 [First Modification of Second Embodiment]

A printed circuit board 120 according to the first modification of the second embodiment of the present invention will be described hereinafter with reference to Fig. 19. In the second embodiment stated above, a PGA method for establishing 15 connection through the conductive connection pins 178 as shown in Fig. 13 has been described. The first modification of the second embodiment is almost the same in constitution as the second embodiment except that bumps 176 at a daughter board side are connected to the daughter board by a BGA method.

20 Now, a method of manufacturing a printed circuit board according to the first modification of the second embodiment will be described with reference to Figs. 14 to 19.

(1) A copper-clad laminated plate 130A having copper foils 132 each having a thickness of 18 μm and laminated on the both 25 sides of a substrate 130 having a thickness of 1 mm and made of a glass epoxy resin or a BT (Bismaleimide-Triazine) resin is employed as a starting material (Fig. 14(A)). First, this

copper-clad laminated plate 130A is drilled and then a plating resist is formed. Thereafter, the substrate 130 is subjected to an electroless copper plating process to form through holes 136 and the copper foils 132 are etched in a pattern fashion 5 according to an ordinary method, thereby forming lower conductor circuits 134 on both sides of the substrate 130 (Fig. 14(B)).

(2) After washing and drying the substrate 130 on which the lower conductor circuits 134 have been formed, an etching solution is sprayed on the both sides of the substrate 130 and 10 the surfaces of the lower conductor circuits 134, the inner walls of the through holes 136 and the surfaces of lands 136a are etched, thereby forming rough layers 134a and 136a on the entire surfaces of the lower conductor circuits 134 including the through holes 136 (Fig. 14(C)). As the etching solution, a solution mixture 15 of 10 parts by weight of imidazole copper (II) complex, 7 parts by weight of a glycolic acid, 5 parts by weight of potassium chloride and 78 parts by weight of ion-exchange water is employed. The roughing process may be performed by conducting soft etching, by conducting a blackening (oxidization)-reduction process or 20 by forming a needle alloy plated material (Interplate manufactured by EBARA UDYLITE Co., Ltd.) consisting of copper-nickel-phosphorous or the like.

(3) Next, the surfaces of the lands 136a of the through holes 136 having the rough layers 136a formed thereon, respectively, 25 are polished by buffing to flatten the surfaces of the lands 136a (Fig. 14(D)).

(4) Next, a mask 139 having opening portions 139a corresponding

to the respective through holes 136 is mounted on the substrate 130 and resin filler 154 mainly consisting of an epoxy resin is applied using a printer (Fig. 15(A)). In the step of (3), after forming the rough layers 136a on the through holes 136, 5 the surfaces of the lands 136a of the through holes 136 are polished and flattened. Due to this, when filling the resin filler in the through holes 136, it is possible to prevent the resin filler 154 from flowing out along the rough layers (anchors) formed on the lands 136a of the thorough holes 136. It is, therefore, 10 possible to form the filler 154 in the through holes flat and to enhance the reliability of wirings above the through holes to be formed in a step described later.

Thereafter, using the printer, the resin filler 154 mainly consisting of an epoxy resin is applied onto the both sides of 15 the substrate 130 and dried. Namely, through this step, the resin filler 154 is filled between the lower conductor circuits 134 (Fig. 15(B)). As the resin filler 154, it is preferable to employ one selected from a mixture of an epoxy resin and organic filler, a mixture of an epoxy resin and inorganic filler and 20 a mixture of an epoxy resin and inorganic fiber. Alternatively, the resin filler in the first embodiment may be employed.

(5) One side of the substrate 130 for which the process described in (4) above has been completed, is polished by belt sander polishing using belt abrasive paper (manufactured by 25 Sankyo) in such a manner that the resin filler 154 is not left on the surfaces of the lower conductor circuits 134 and those of the lands 136a of the through holes 136. Then, buffing is

performed to remove flaws caused by the belt sander polishing. These series of polishing are also conducted to the other side of the substrate 130. The resin filler 154 thus filled is thermally hardened (Fig. 15(C)).

5 (6) Next, the same etching solution as that employed in (2) above is sprayed on the both sides of the substrate 130 for which the process described in (5) above has been completed and the surfaces of the lower conductor circuits 134 and those of the lands 136a of the through holes 136 which have been flattened 10 once are etched, thereby forming rough surfaces 134a on the entire surfaces of the lower conductor circuits 134 (Fig. 15(D)).

(7) Then, thermosetting cycloolefin resin sheets each having a thickness of 50 μm are laminated by vacuum pressing while raising a temperature to 50 to 150 $^{\circ}\text{C}$ and at a pressure of 5 kg/cm^2 to 15 thereby provide interlayer resin insulating layers 150 each consisting of a cycloolefin resin (Fig. 16(A)). The degree of vacuum during vacuum pressing is 10 mmHg. Alternatively, the resin films employed in the second embodiment may be employed instead of the above resin sheets.

20 (8) Next, via hole openings 152 each having a diameter of 80 μm are formed on the interlayer resin insulating layers 150 through masks 151 each having a thickness of 1.2 mm and having penetrating holes 151a formed therein, by using CO_2 gas laser at a wavelength of 10.4 μm on conditions of a beam diameter of 25 5 mm, a top-hat mode, a pulse width of 50 microseconds, the diameter of each hole of the masks of 0.5 mm and three shots (Fig. 16(B)). Then, a de-smear process is performed using oxygen plasma.

(9) Then, using SV-4540 manufactured by ULVAC JAPAN, Ltd., a plasma process is performed to rough the surfaces of the interlayer resin insulating layers 150, thereby forming rough surfaces 150 α (Fig. 16(C)). The plasma process is performed 5 for two minutes while using, as inert gas, argon gas on conditions of power of 200 W, a gas pressure of 0.6 Pa and a temperature of 70°C. Alternatively, the rough surfaces may be formed by using an acid or an oxidizer.

(10) Next, using the same device, the argon gas contained inside 10 is exchanged and sputtering is conducted with Ni and Cu as targets, on conditions of an atmospheric pressure of 0.6 Pa, a temperature of 80°C, power of 200 W and a duration of 5 minutes, thereby forming Ni/Cu metal layers 148 on the surfaces of the respective interlayer resin insulating layers 150. At this time, the 15 thickness of each Ni/Cu metal layer 148 is 0.2 μ m (Fig. 16(D)). Electroless copper plated films may be further formed on the layers 148, respectively, instead of conducting sputtering.

(11) Next, commercially available photosensitive dry films are bonded onto the both sides of the substrate 130 for which the 20 above process has been completed. Photomask films are mounted, exposed with 100 mJ/cm² and developed with a 0.8% sodium carbonate solution, thereby forming plating resists 155 each having a thickness of 15 μ m. Then, the substrate 130 is subjected to electroplating on the following conditions, thereby forming 25 electroplated films 157 each having a thickness of 15 μ m (Fig. 17(A)). It is noted that an additive in the electroplating solution is Kaparacid HL manufactured by Atotech Japan.

[Electroplating Solution]

Sulfuric acid	2.24 mol/l
Copper sulfate	0.26 mol/l
Additive	19.5 mol/l

[Electroplating Conditions]

Current density	1 A/dm ²
Duration	65 minutes
temperature	22±2°C

5 (12) After separating and removing the plating resists 155 with 5% NaOH, the Ni/Cu metal layers 148 existing below the plating resists 155 are dissolved and removed by performing etching with a solution mixture of a nitric acid, a sulfuric acid and hydrogen peroxide, thereby forming conductor circuits 145 (including via 10 holes 146) each consisting of the electroplated copper film 157 and the like and having a thickness of 16 µm (Fig. 17(B)).

(13) Next, the same etching process as that in the step of (6) is performed to form rough surfaces 145a on the conductor circuits 145, respectively (Fig. 17(C)).

15 (14) By repeating the steps of (7) to (13) above, interlayer resin insulating layers 160 and conductor circuits 165 (including via holes 166) are formed further above (Fig. 17(D)).

(15) Next, a solder resist composition (organic resin insulating material) prepared in the same manner as that in the 20 first embodiment is obtained.

(16) The solder resist composition is applied to each side of

the substrate 130 to have a thickness of 20 μm and dried. Then, a photomask is closely attached to each solder resist layer 170, exposed to ultraviolet rays, developed with a DMTG solution to thereby form openings 171 each having a diameter of 200 μm .

5 Thereafter, a heating process is performed to harden the solder resist layers 170 to thereby provide the solder resist layers 170 each having openings 171 and having a thickness of 20 μm (Fig. 18(A)).

(17) The substrate 130 having the solder resist layers 170 formed thereon is immersed in an electroless nickel plating solution to form nickel plated layers 172 each having a thickness of 5 μm in the respective openings 171. Further, the substrate 130 is immersed in an electroless plating solution to thereby form gold plated layers 174 each having a thickness of 0.03 μm 15 on the respective nickel plated layers 172 (Fig. 18(B)).

(18) Then, a solder paste is printed on each opening 171 of the solder resist layers 170 and a reflow process is performed at 200°C to form solder bumps 176, thus manufacturing a printed circuit board 120 having the solder bumps 176 (Fig. 19).

20

[Second Modification of Second Embodiment]

A printed circuit board according to the second modification is almost the same as the printed circuit board in the first embodiment described above with reference to Figs. 25 1 to 6. However, in the second modification, as shown in Fig. 20(A), after rough layers (made of an alloy consisting of Cu-Ni-P) 47 are formed on via holes 46 and through holes 36, respectively,

by electroless plating, the lands 136a of the through holes 36 on which the rough layers 47 have been formed, respectively, are polished by buffing and flattened (Fig. 20(B)). Thereafter, resin filler 54 is filled in the through holes 36 and the via holes 46 through masks and dried (Fig. 20(C)). By doing so, it is possible to prevent the resin filler 54 from flowing out along the rough layers 47.

[Comparison Example 5]

10 A printed circuit board in a comparison example 5 is basically the same as the printed circuit board in the second embodiment except that the land surfaces of through holes having rough layers formed thereon, respectively, are not polished nor flattened but resin filler is filled in the through holes. The 15 remaining conditions are the same as those in the second embodiment.

[Comparison Example 6]

20 A printed circuit board in a comparison example 6 is basically the same as the printed circuit board in the first modification of the second embodiment except that the land surfaces of through holes having rough layers formed thereon, respectively, are not polished nor flattened but resin filler is filled in the through holes. The remaining conditions are 25 the same as those in the first modification of the second embodiment.

[Comparison Example 7]

A printed circuit board in a comparison example 7 is basically the same as the printed circuit board in the second modification of the second embodiment except that the land surfaces of through holes having rough layers formed thereon, respectively, are not polished nor flattened but resin filler is filled in the through holes. The remaining conditions are the same as those in the second modification of the second embodiment.

The printed circuit boards in the second embodiment, the first modification and the second modification of the second embodiment were compared with the printed circuit boards in the comparison examples in respect of three points, i.e., the roughing method, the surface polishing of the lands of the through holes and the flow of the resin filler out of the through holes. The comparison result is shown in Fig. 21. As is obvious from the result shown in Fig. 21, in the printed circuit boards in the comparison examples 5, 6 and 7, the resin filler flowed out along the rough layers formed on the lands of the through holes when filling the resin filler in the through holes because the surfaces of the lands of the through holes having the rough layers formed thereon, respectively, were not polished.

WHAT IS CLAIMED IS:

1. A multi-layer printed circuit board having buildup layers formed on both sides of a core substrate, the buildup layers each having interlayer resin insulating layers and conductive layers alternately provided, the conductor layers connected to one another by via holes, wherein

through holes are formed to penetrate said core substrate and the interlayer resin insulating layers formed on the both sides of the core substrate; and

10 the via holes are formed right on said through holes, the via holes connected to external connection terminals.

2. A multi-layer printed circuit board according to claim 1, wherein

resin filler is filled in said through holes and the conductor layers are formed to cover exposed surfaces of the resin filler from the through holes; and

the via holes right on said through holes are formed on said conductor layers of said through holes.

3. A method of manufacturing a multi-layer printed circuit board comprising at least the following steps (a) to (d):

(a) forming lower interlayer resin insulating layers on both sides of a core substrate, respectively;

(b) forming through holes penetrating said core substrate and said lower interlayer resin insulating layers;

25 (c) forming upper interlayer resin insulating layers on said lower interlayer resin insulating layers, respectively; and

(d) forming via holes in said upper interlayer resin insulating layers, the via holes connected to external connection terminals and formed right on part of said through holes.

4. A method of manufacturing a multi-layer printed circuit board comprising at least the following steps (a) to (g):

(a) forming lower interlayer resin insulating layers on both sides of a core substrate, respectively;

(b) forming through holes penetrating said core substrate and said lower interlayer resin insulating layers;

10 (c) filling resin filler in said through holes;

(d) polishing and flattening the resin filler pouring from said through holes;

(e) forming conductor layers covering exposed surface of said resin filer from said through holes;

15 (f) forming upper interlayer resin insulating layers
on said lower interlayer resin insulating layers, respectively;
and

(g) forming via holes in said upper interlayer resin insulating layers and forming the via holes right on part of
20 said through holes so as to be connected to external connection terminals.

5. A multi-layer printed circuit board having interlayer resin insulating layers on both sides of a core substrate, respectively, through holes provided to penetrate the core substrate and filled with resin filler, the interlayer resin insulating layers and conductor circuits provided, wherein
25 said resin filler contains an epoxy resin, a curing agent

and 10 to 50% of inorganic particles.

6. A multi-layer printed circuit board having interlayer resin insulating layers formed on both sides of a core substrate, respectively, through holes provided to penetrate the core substrate and filled with resin filler, plated covers provided, the interlayer resin insulating layers and conductor circuits provided, wherein

 said resin filler contains an epoxy resin, a curing agent and 10 to 50% of inorganic particles.

10 7. A multi-layer printed circuit board according to claim 5 or 6, wherein

 said inorganic particles contain one type or more selected from a group consisting of aluminum compounds, calcium compounds, potassium compounds, magnesium compounds and silicon compounds.

15 8. A multi-layer printed circuit board according to claim 6 or 7, wherein

 a shape of said inorganic particles is one of a spherical shape, a circular shape, an ellipsoidal shape, a pulverized shape and a polygonal shape.

20 9. A multi-layer printed circuit board according to any one of claim 6 to 8, wherein

 rough layers are provided on the conductor layers of said through holes, respectively.

10. A method of manufacturing a multi-layer printed circuit board having interlayer resin insulating layers provided on both sides of a core substrate, for forming the interlayer resin insulating layers through the following steps (a) to (e):

- (a) a formation step of forming through holes penetrating the both sides of the printed circuit board;
- (b) a filling step of filling resin filler containing an epoxy resin and 10 to 50% of inorganic particles;
- (c) a drying step and a polishing step;
- (d) a hardening step; and
- (e) a cover plating step.

11. A method according to claim 10, wherein
in said polishing step (c), a buffing step is conducted
at least once or a plurality of times.

10 at least once or a plurality of times.

12. A method according to claim 10 or 11, wherein
in said step (a), a step of forming rough layers is
conducted.

13. A multi-layer printed circuit board having buildup layers
15 on both sides of a core substrate, respectively, said buildup
layer having interlayer resin insulating layers and conductor
layers alternately provided, the conductor layers connected to
one another by via holes, wherein

through holes filled with resin filler are formed to
20 penetrate said core substrate and lower interlayer resin
insulating layers formed on the both sides of the core substrate;
and

via holes filled with said resin filler are formed in said lower interlayer resin insulating layers.

25 14. A multi-layer printed circuit board according to claim
13, wherein

the conductor layers are formed to cover exposed surfaces

of the resin filler filled in the via holes of said lower interlayer resin insulating layers; and

via holes are formed right on the via holes through the conductive layers, respectively.

5 15. A method of manufacturing a multi-layer printed circuit board comprising at least the following steps (a) to (g):

(a) forming lower interlayer resin insulating layers on both sides of a core substrate, respectively;

10 (b) forming penetrating holes in said core substrate and said lower interlayer resin insulating layers, the penetrating holes becoming through holes;

(c) forming openings in said lower interlayer resin insulating layers, the openings becoming via holes;

15 (d) forming conductive films in said penetrating holes and said openings to thereby provide the through holes and the via holes, respectively;

(e) filling resin filler in said through holes and said via holes;

20 (f) polishing and flattening the resin filler pouring out of said through holes and said via holes; and

(g) forming conductor layers covering exposed surfaces of said resin filler from said through holes and said via holes, respectively.

16. A method of manufacturing a multi-layer printed circuit 25 board comprising at least the following steps (a) to (i):

(a) forming lower interlayer resin insulating layers on both sides of a core substrate, respectively;

14
 (b) forming penetrating holes in said core substrate and said lower interlayer resin insulating layers, the penetrating holes becoming through holes;

15 (c) forming openings in said lower interlayer resin insulating layers, the openings becoming via holes;

16 (d) forming conductive films in said penetrating holes and said openings to provide the through holes and the via holes;

17 (e) filling resin filler in said through holes and said via holes;

18 (f) polishing and flattening the resin filler pouring out of said through holes and said via holes;

19 (g) forming conductor layers covering exposed surfaces of said resin filler from said through holes and said via holes;

20 (h) forming upper interlayer resin insulating layers on said lower interlayer resin insulating layers, respectively; and

21 (i) forming via holes in said upper interlayer resin insulating layers and right on part of said via holes.

22 17. A method of manufacturing a multi-layer printed circuit board comprising at least the following steps (a) to (e):

23 (a) forming lower interlayer resin insulating layers on both sides of a core substrate, respectively;

24 (b) forming penetrating holes in said core substrate and said lower interlayer resin insulating layers, the penetrating holes becoming through holes;

25 (c) forming openings in said lower interlayer resin insulating layers, the openings becoming via holes;

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respectively;

(c) polishing and flattening surfaces of lands of said through holes; and

5 (d) filling resin filler in said through holes and forming resin layers.

22. A method according to claim 21, wherein said rough layers are copper oxide layers.

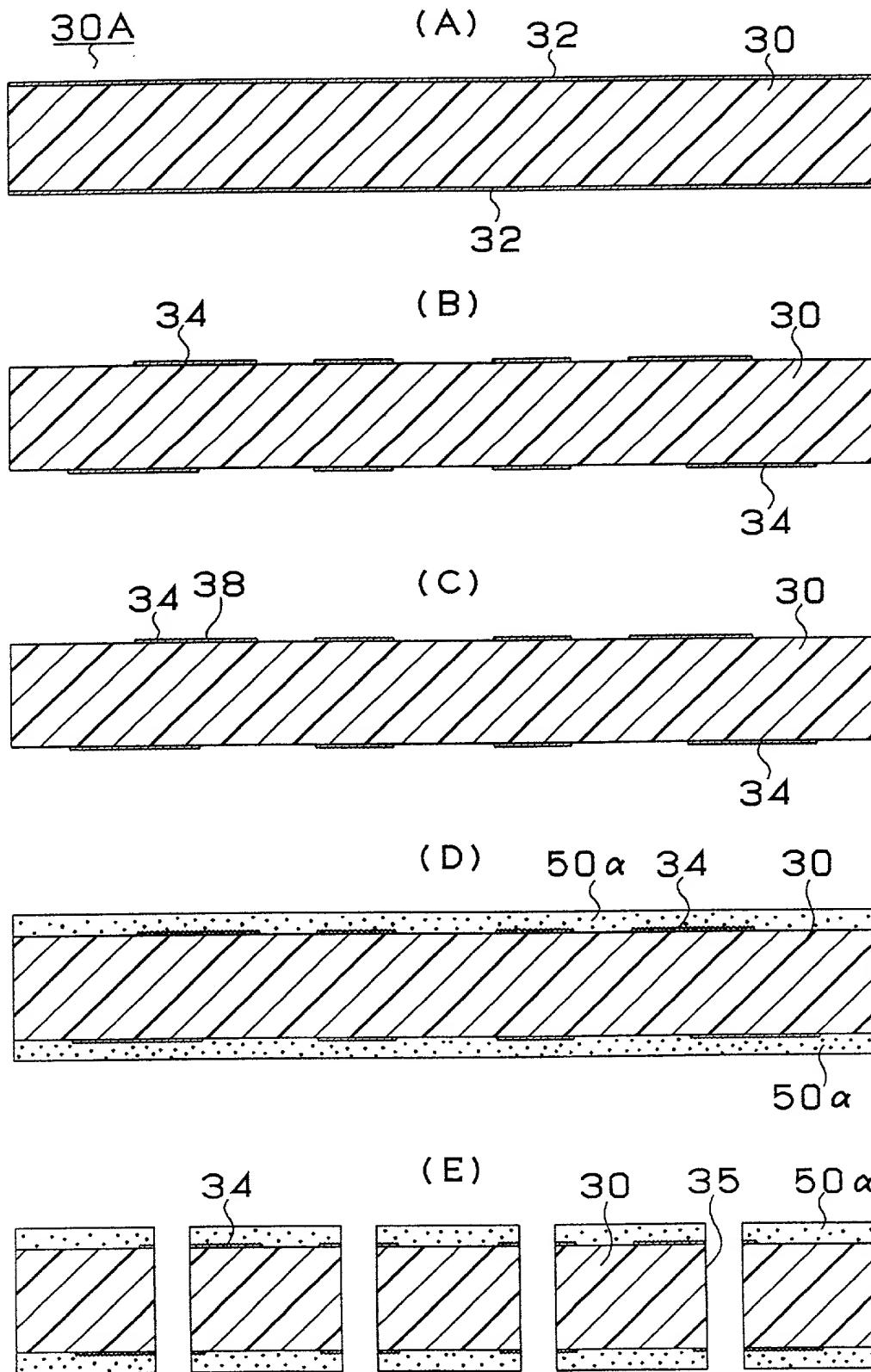
23. A method according to claim 21, wherein said rough layers are formed by etching.

10 24. A method according to claim 21, wherein said rough layers are needle alloy layers made of copper-nickel-phosphorous.

25. A method according to any one of claims 21 to 24, wherein 15 said resin filler is one selected from a group consisting of a mixture of an epoxy resin and organic filler, a mixture of an epoxy resin and inorganic filler and a mixture of an epoxy resin and inorganic fiber.

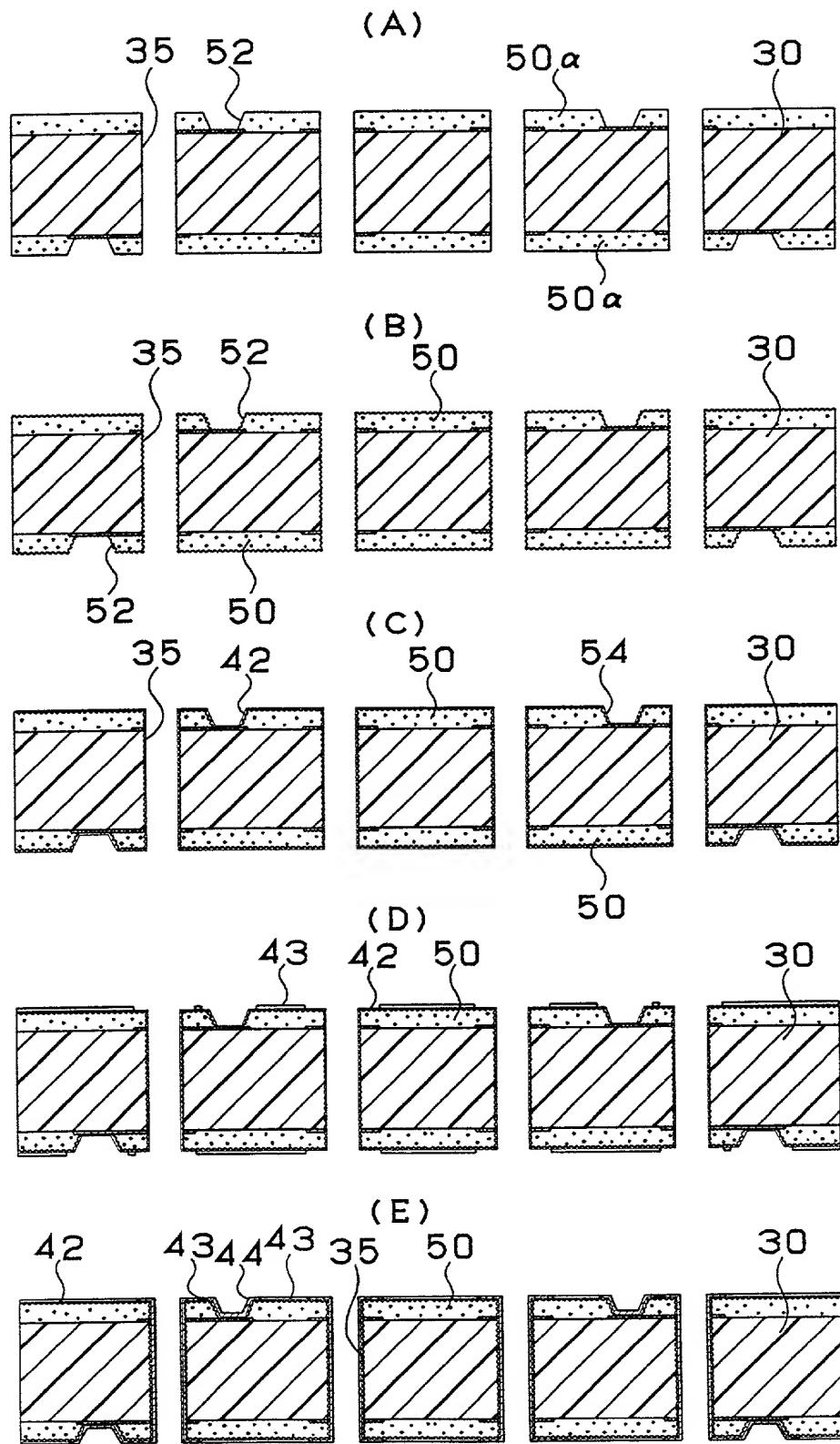
ABSTRACT

Through holes 36 are formed to penetrate a core substrate 30 and lower interlayer resin insulating layers 50, and via holes 66 are formed right on the through holes 36, respectively. Due 5 to this, the through holes 36 and the via holes 66 are arranged linearly, thereby making it possible to shorten wiring length and to accelerate signal transmission speed. Also, since the through holes 36 and the via holes 66 to be connected to solder 10 bumps 76 (conductive connection pins 78), respectively, are directly connected to one another, excellent reliability in connection is ensured.

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Fig. 1

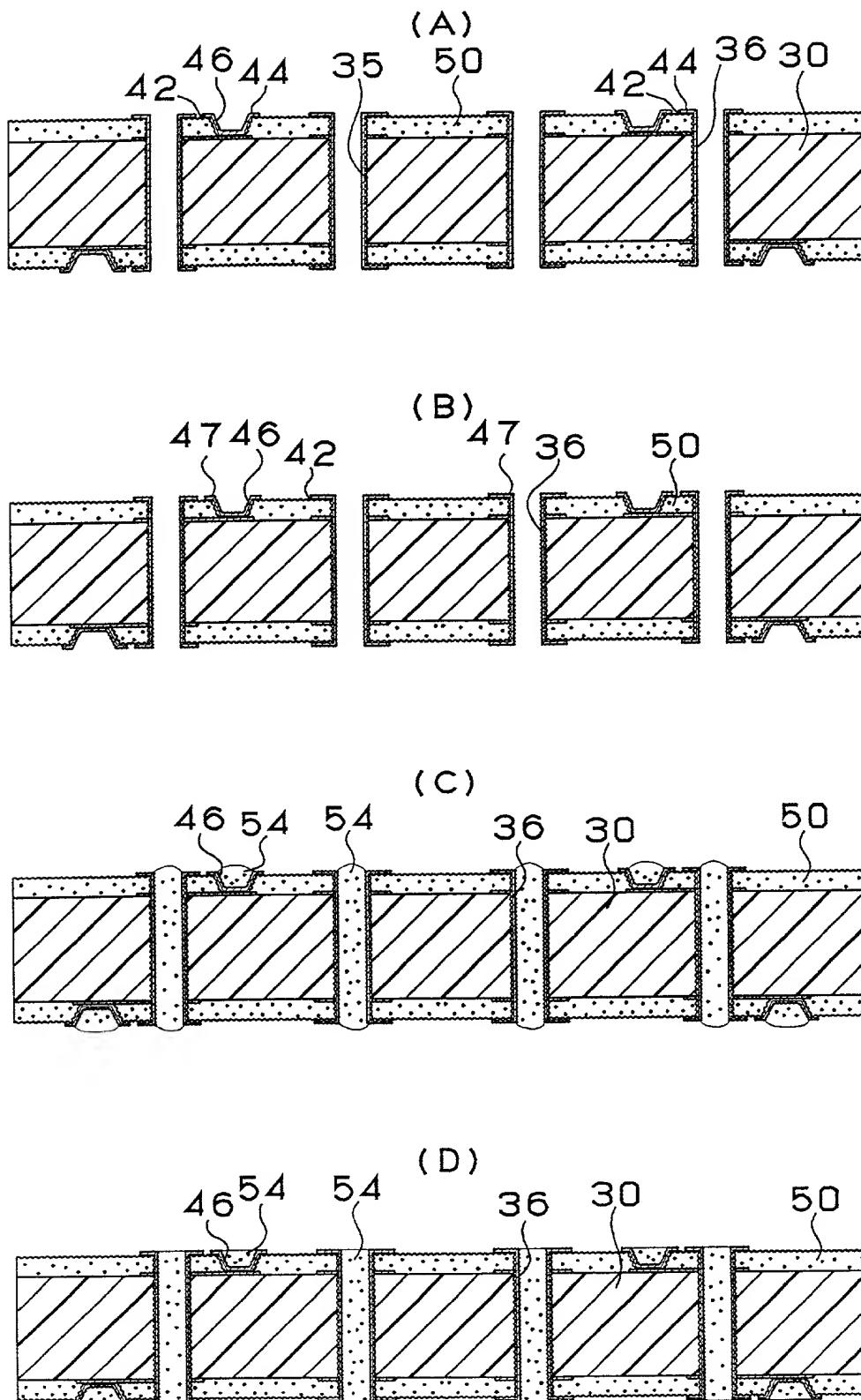
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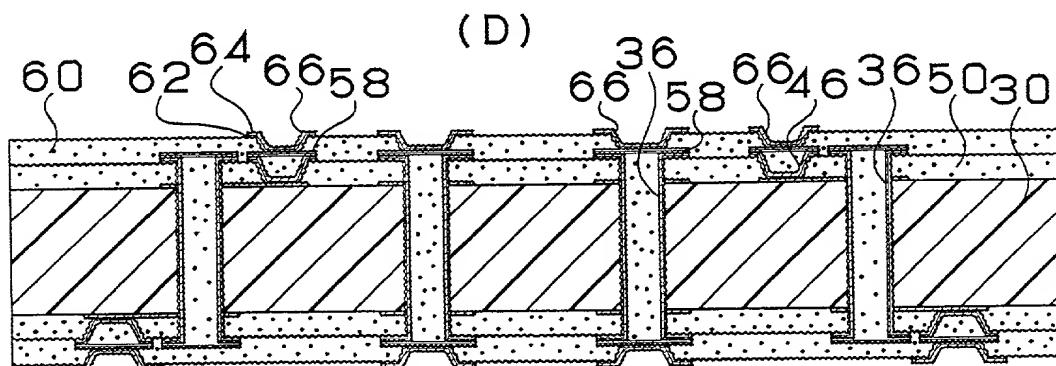
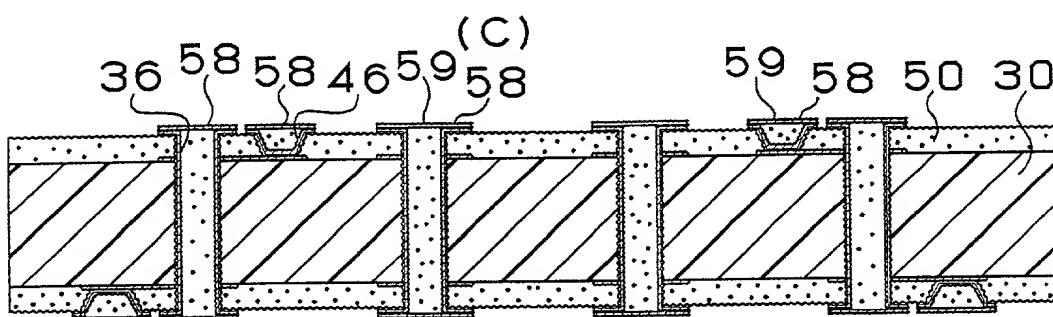
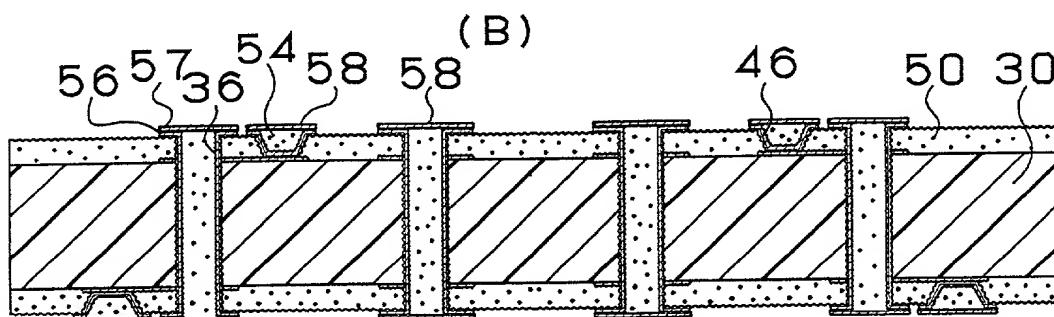
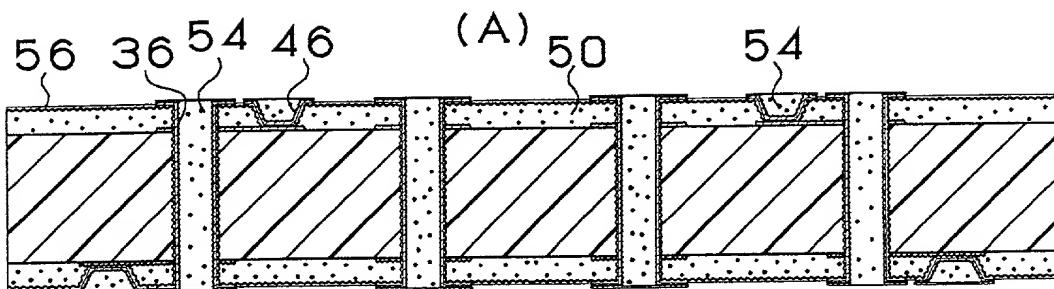
2/22
Fig. 2



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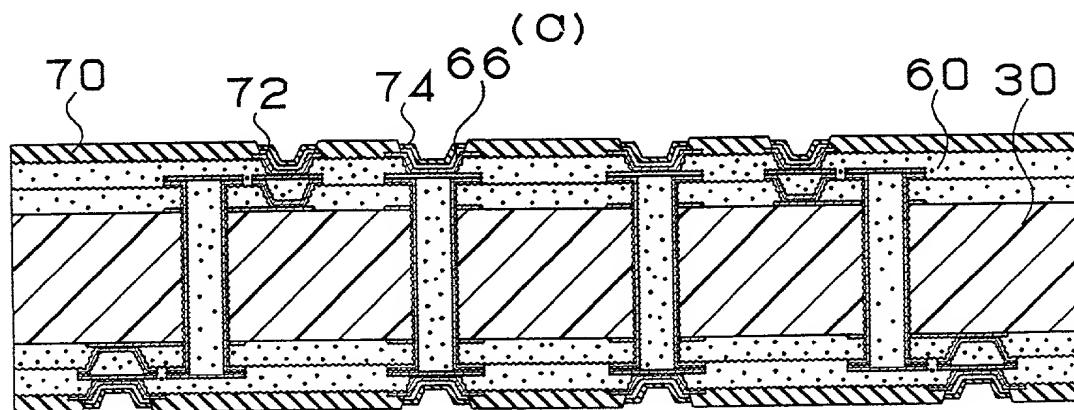
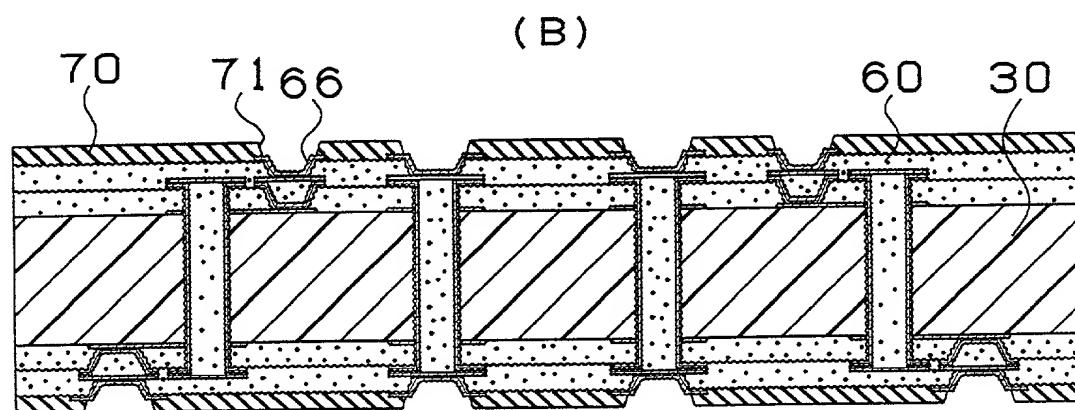
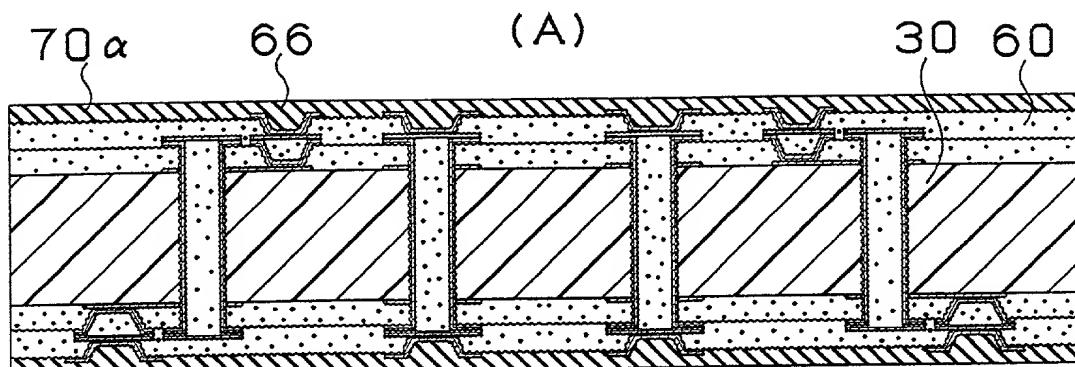
3/22
Fig. 3



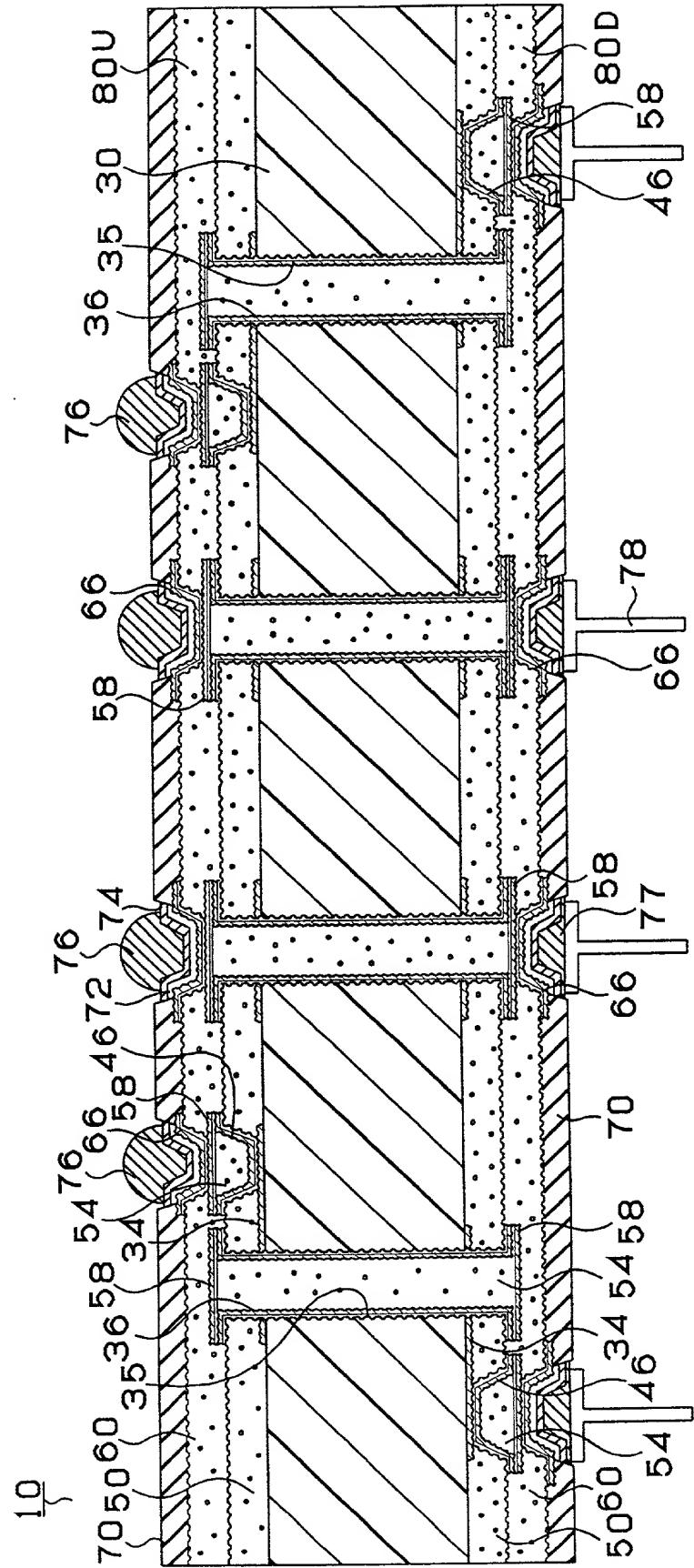
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Fig. 4

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Fig. 5



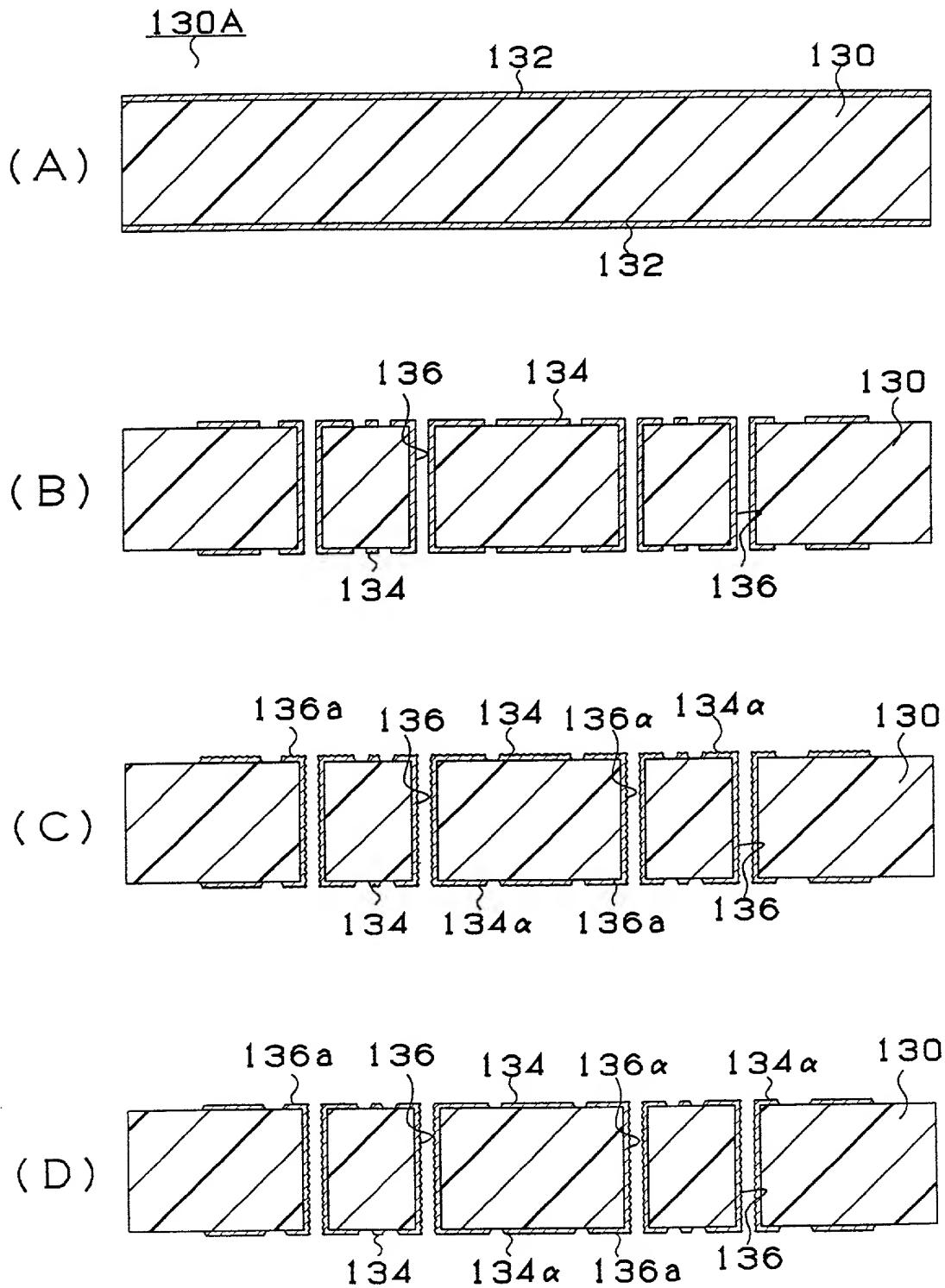
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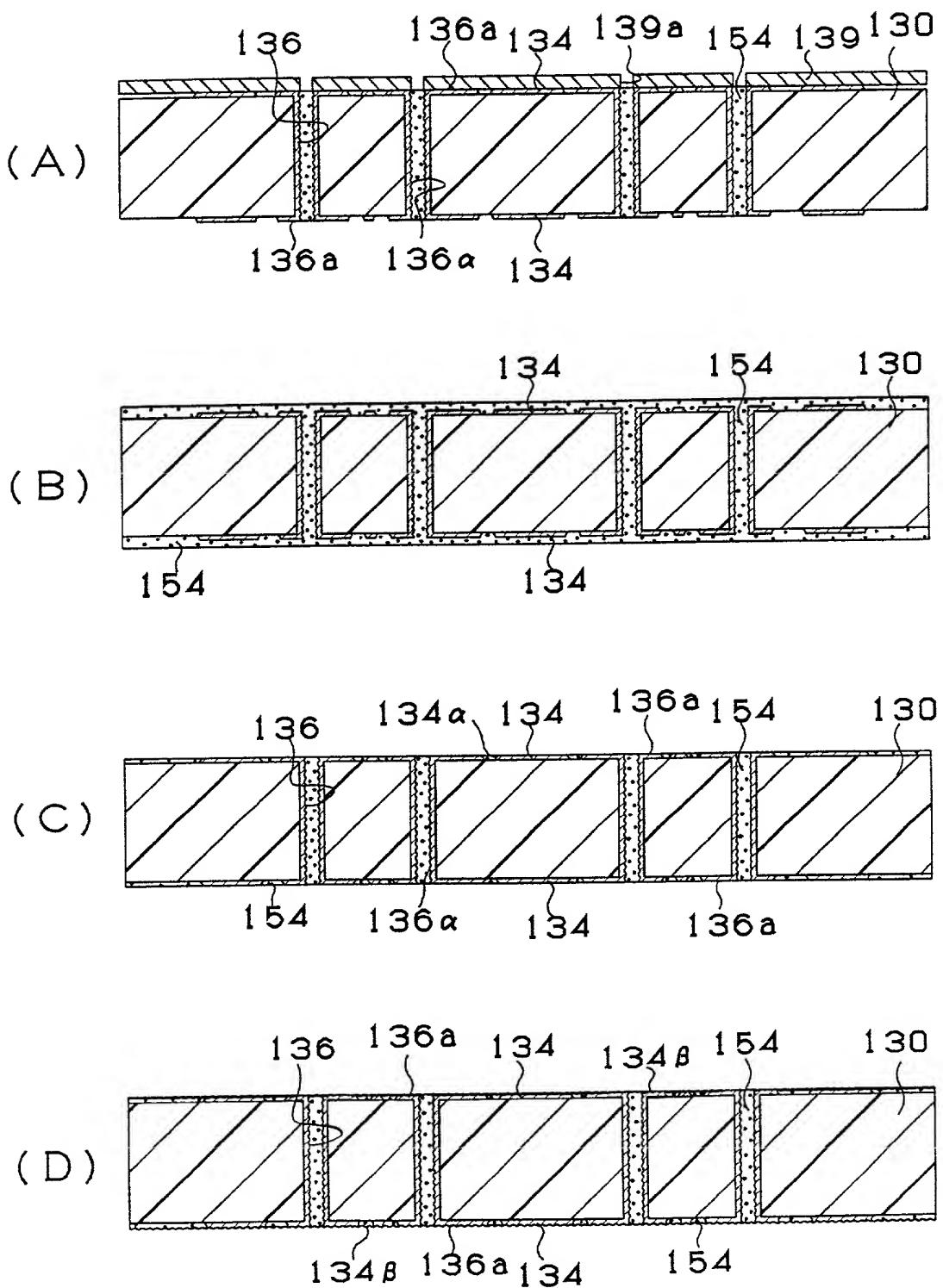
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Fig. 6

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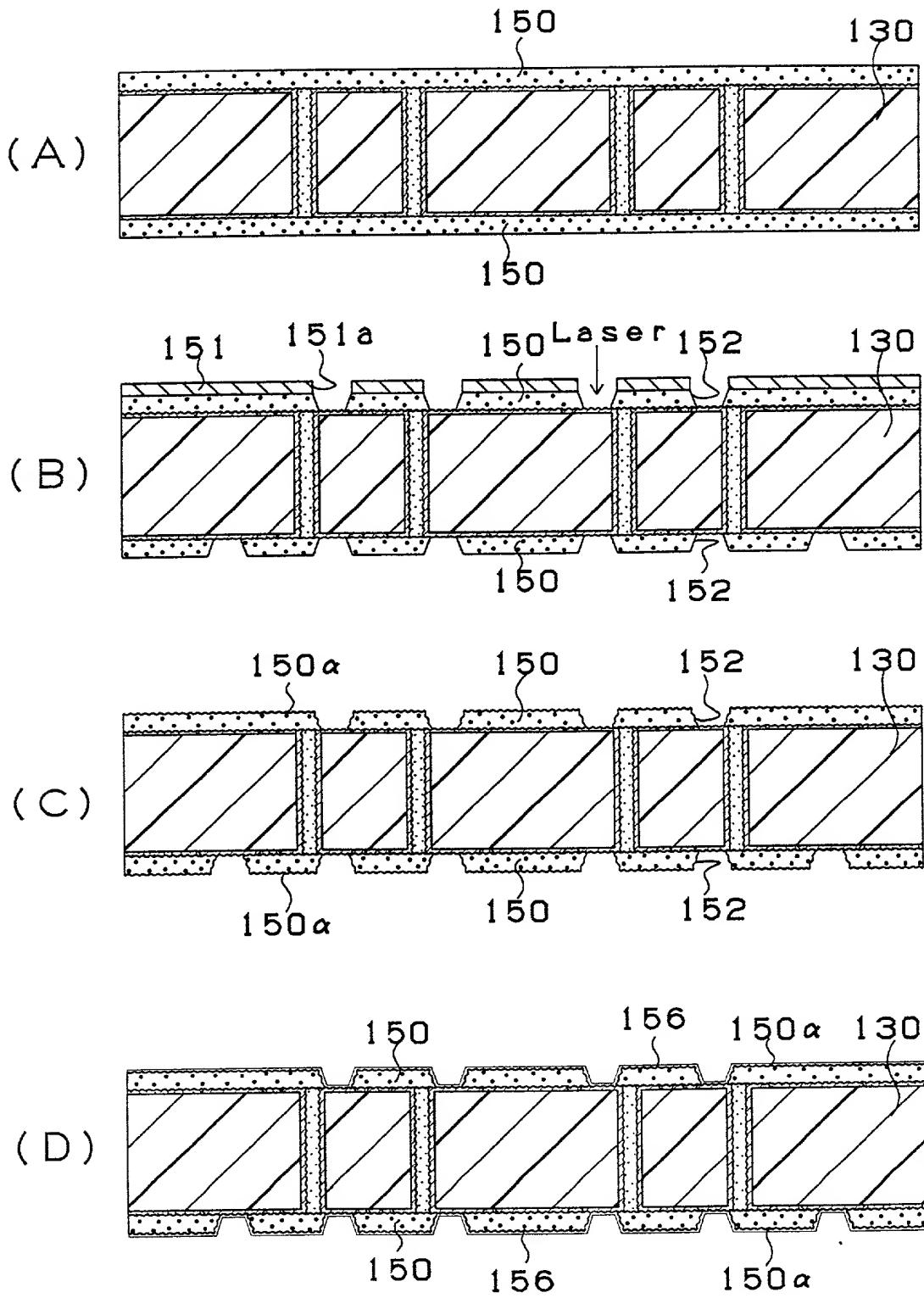
7/22
Fig. 7

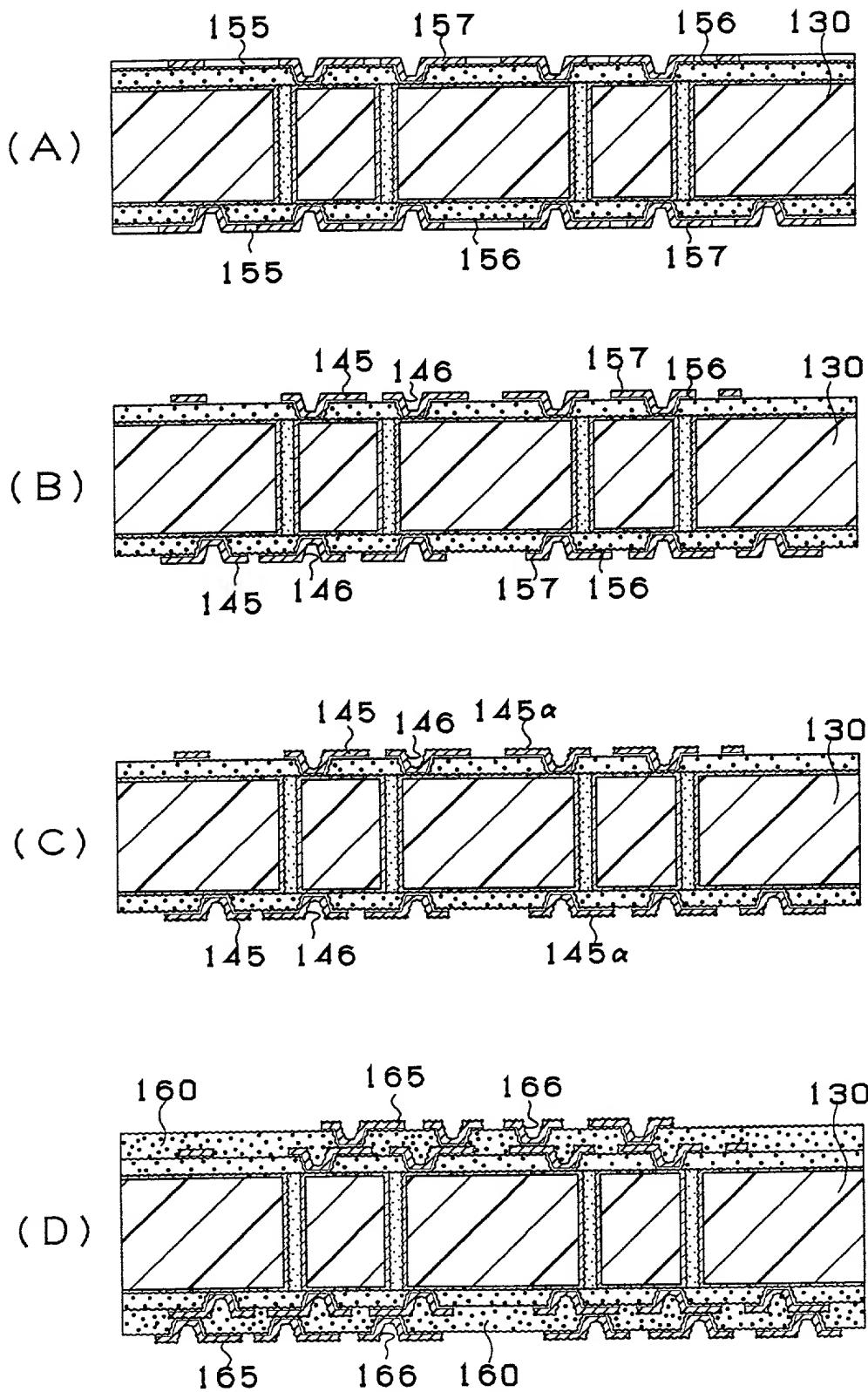
	Embodiment	Comparison Example
Electrical connection characteristic	OK	NG
Separation	NO	YES
Expansion	NO	YES

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Fig. 8

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Fig. 9

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Fig. 10

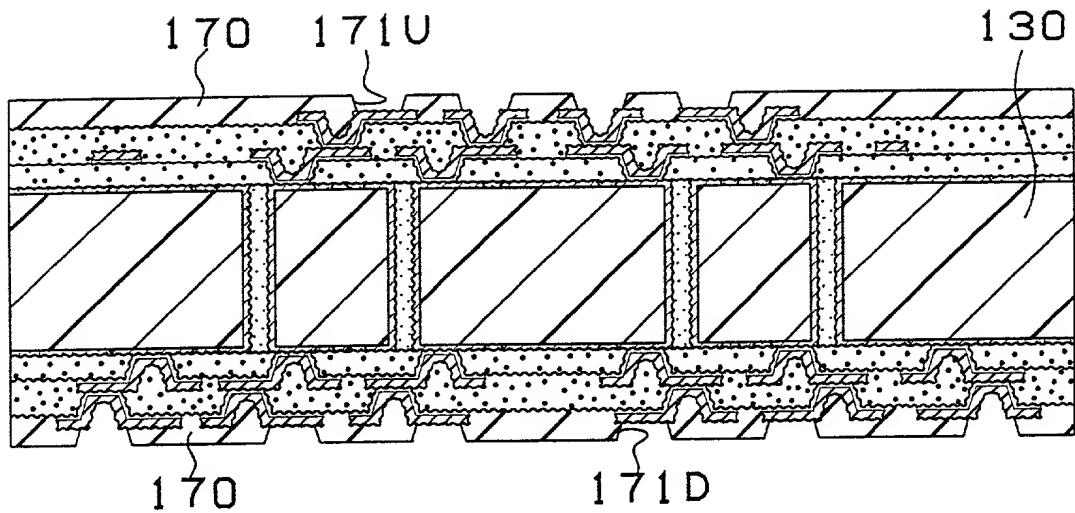
11/22
Fig. 11

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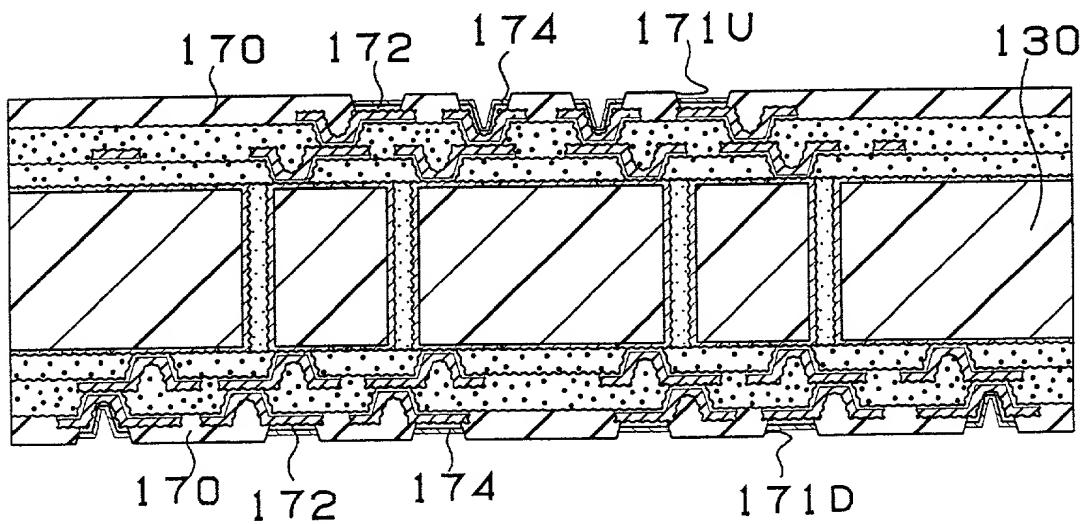
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Fig. 12

(A)



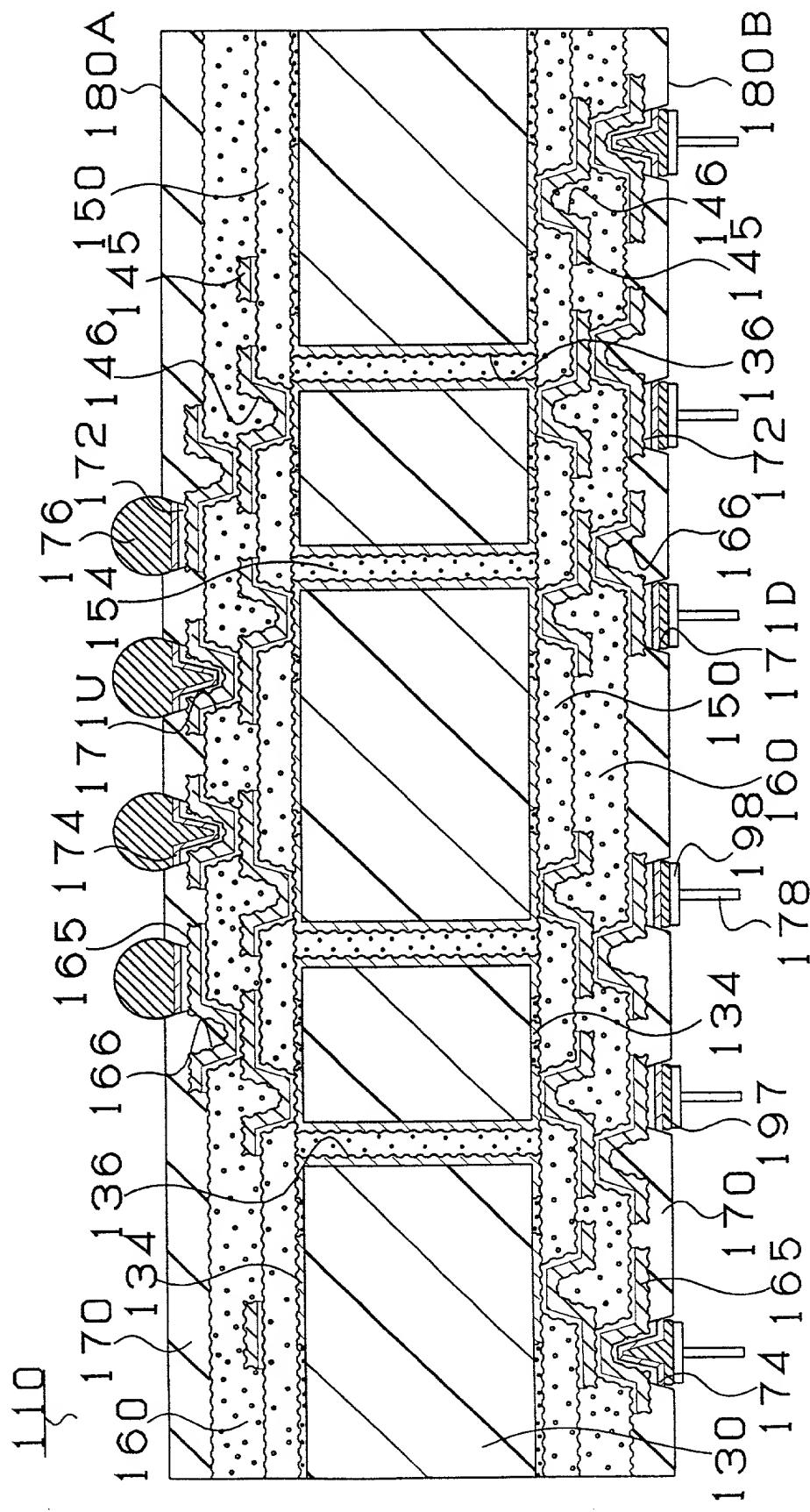
(B)

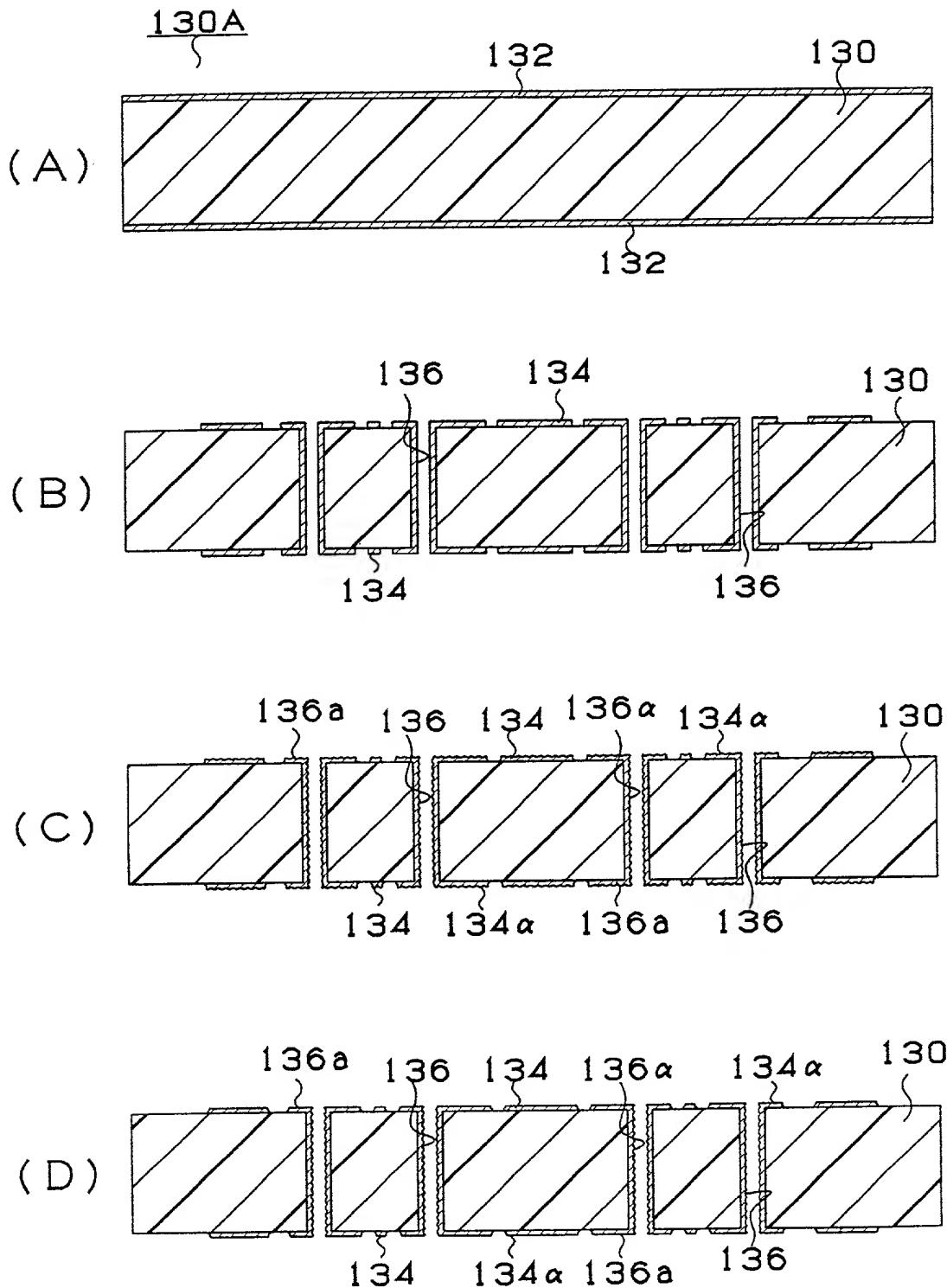


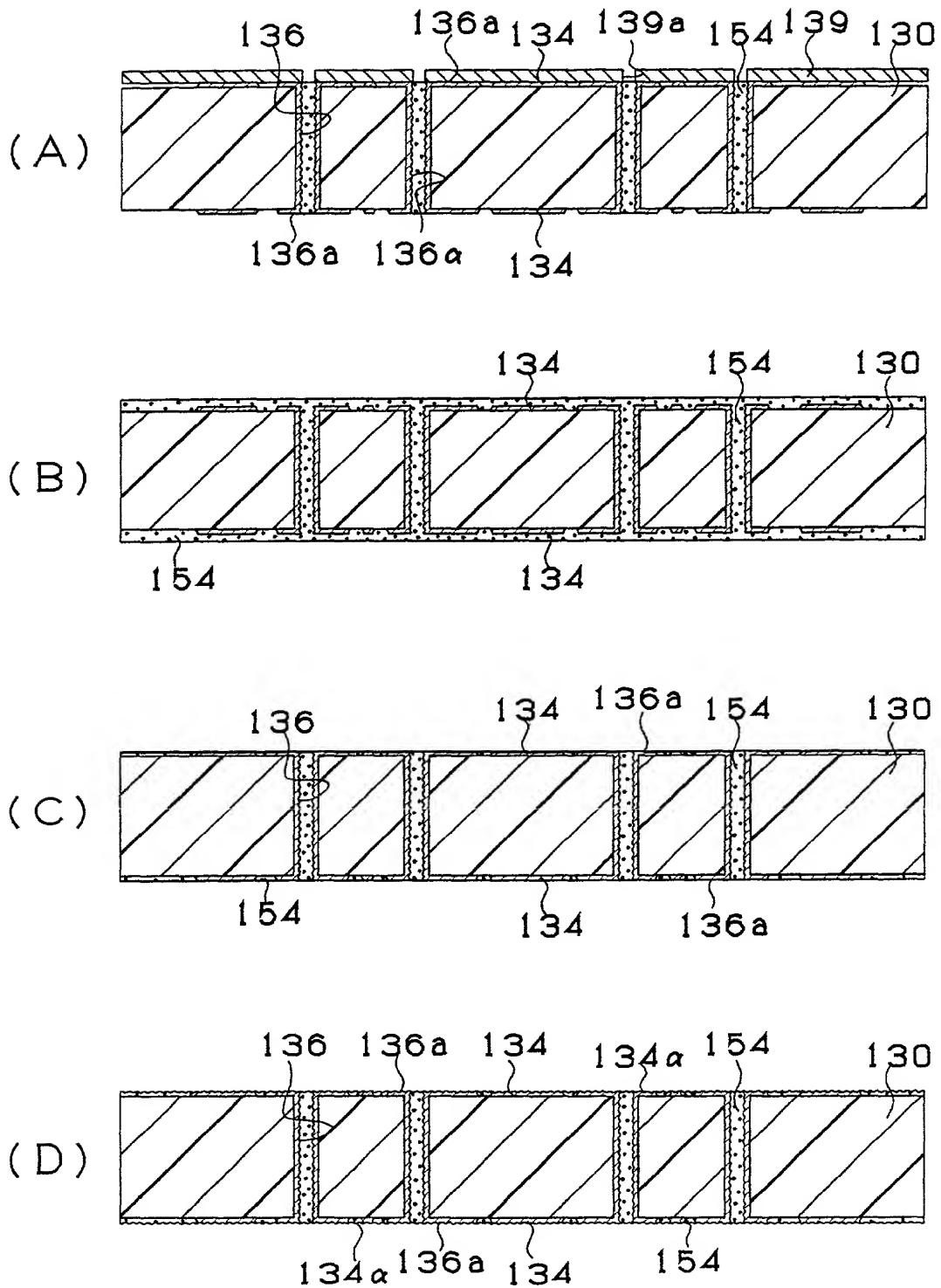
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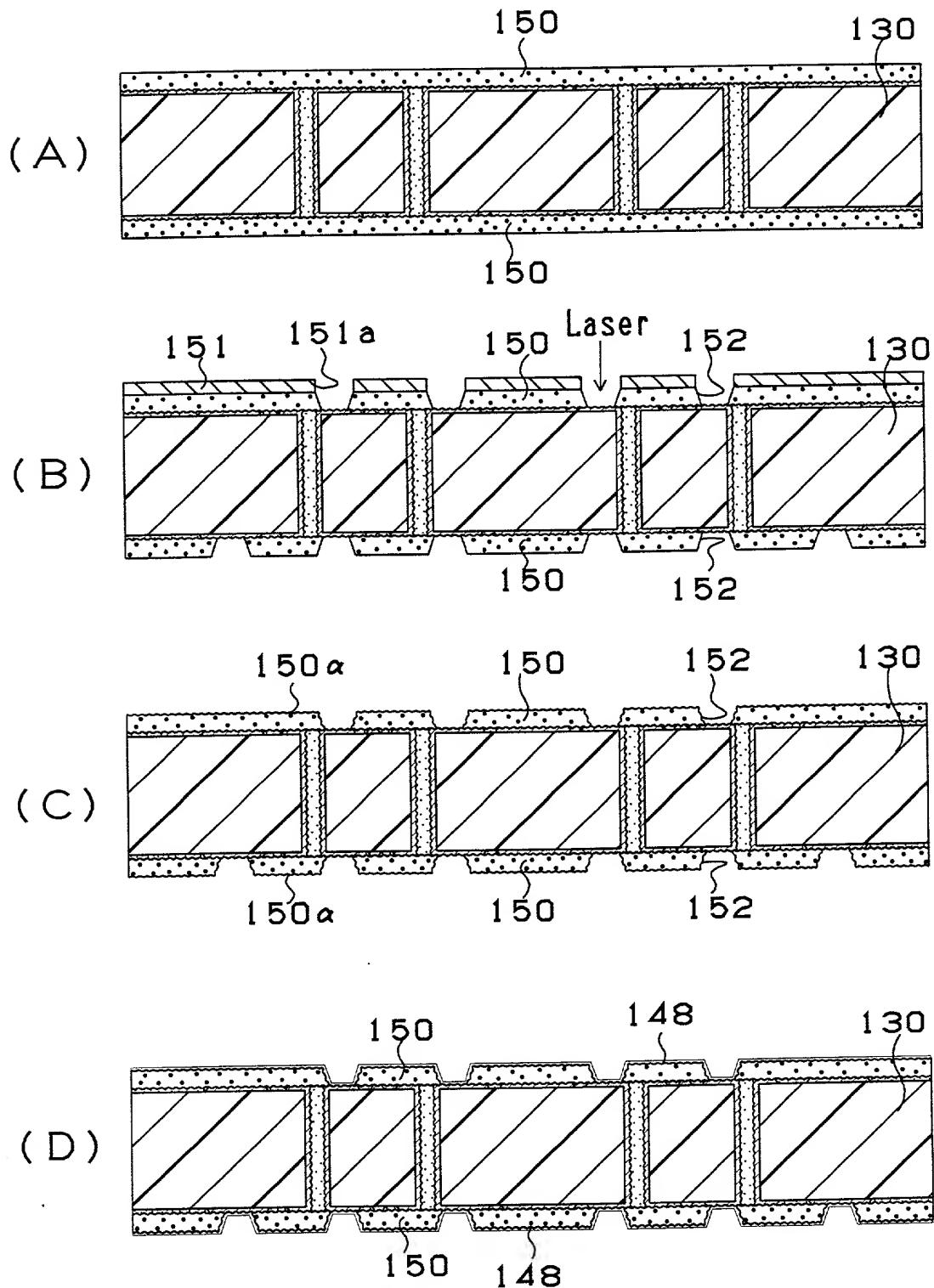
FIGURE 13/22

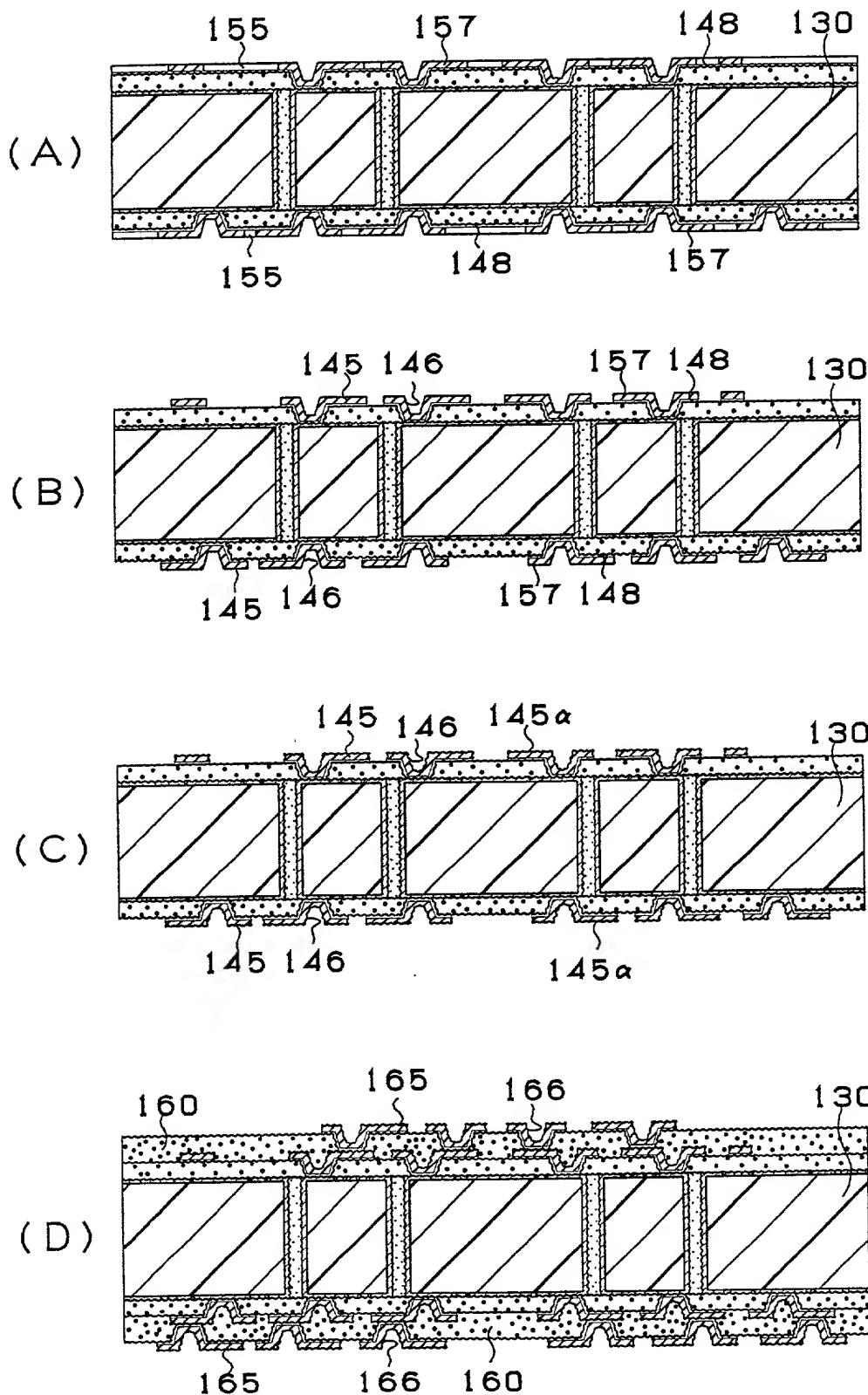
Fig. 13



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Fig. 14

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Fig. 15

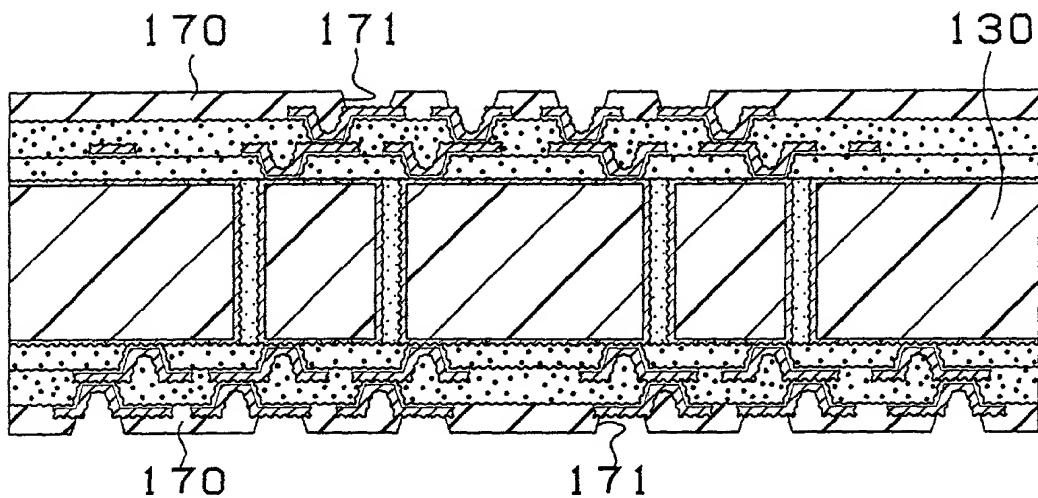
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Fig. 16

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Fig. 17

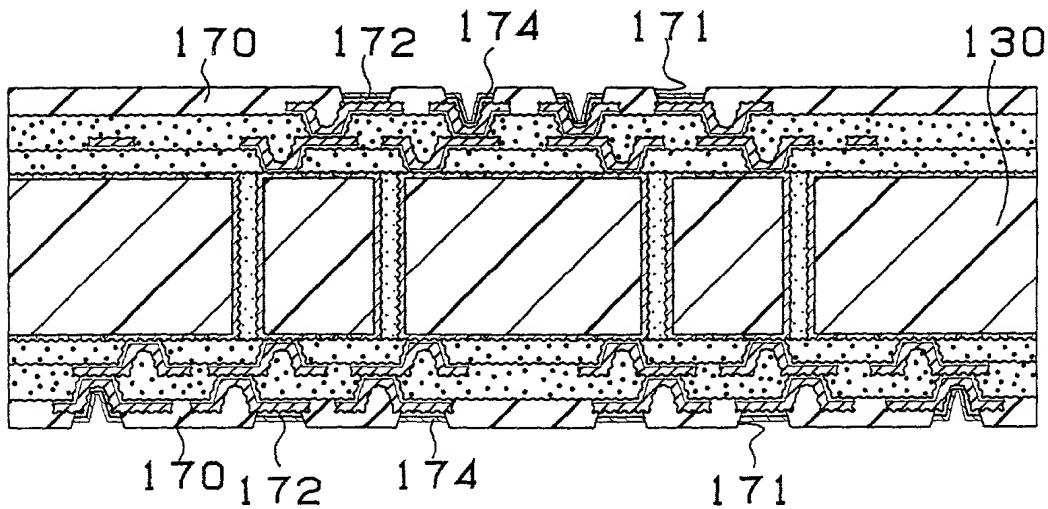
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Fig. 18

(A)

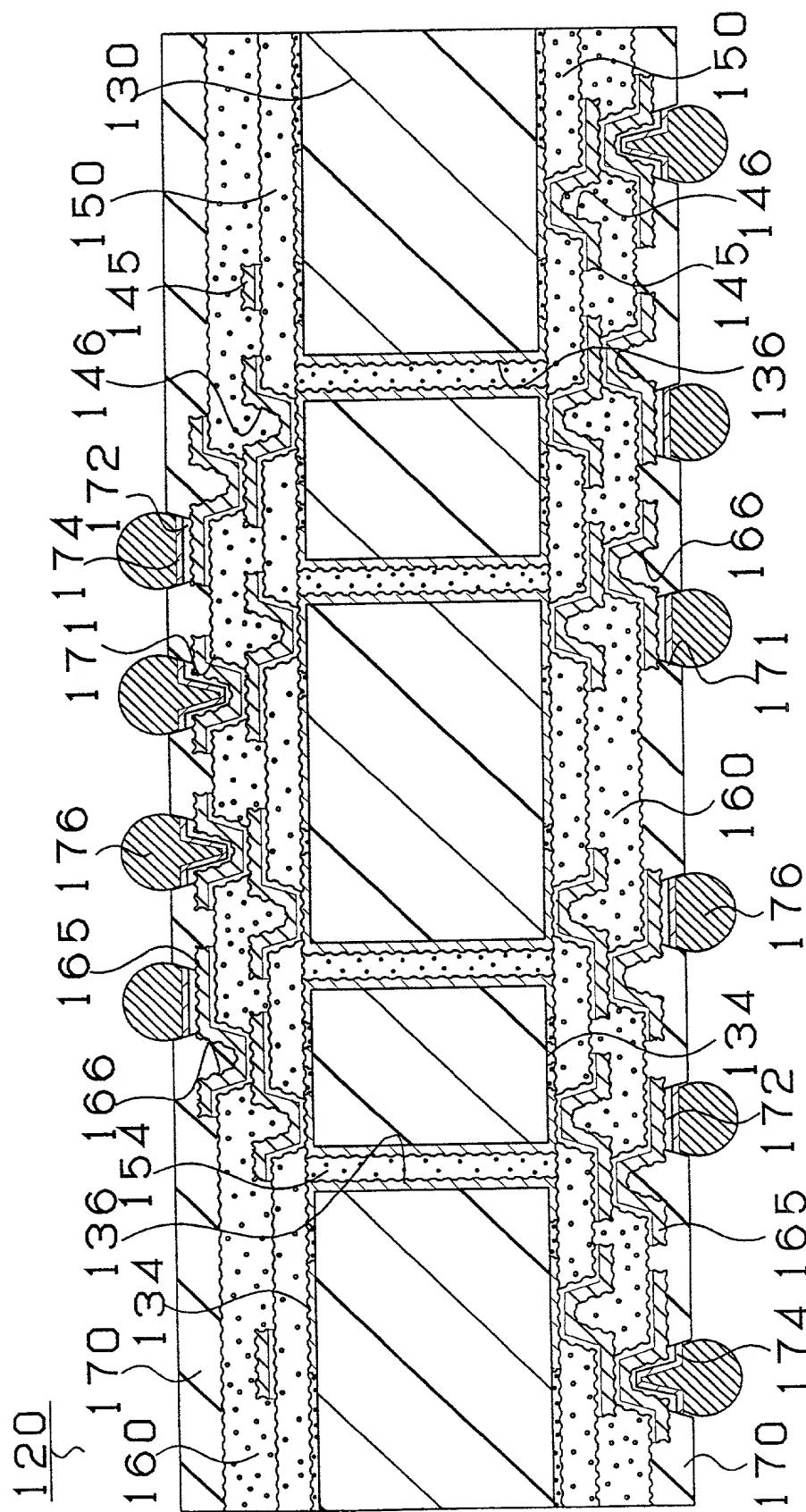


(B)



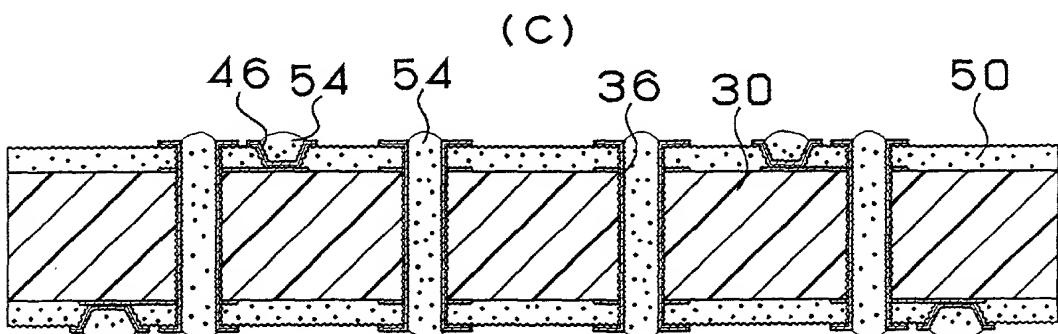
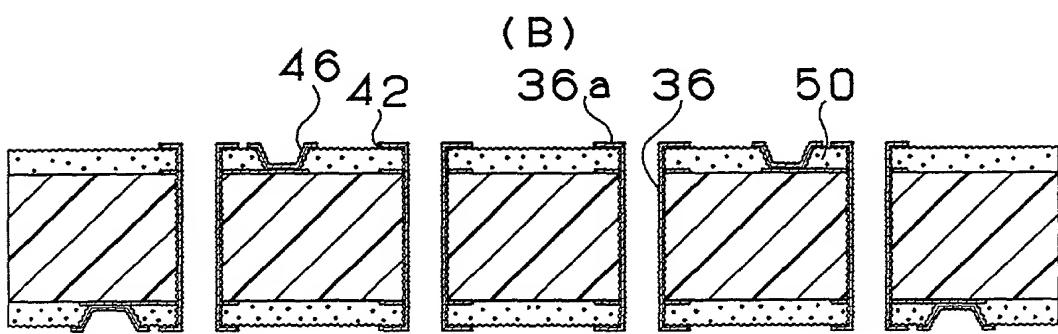
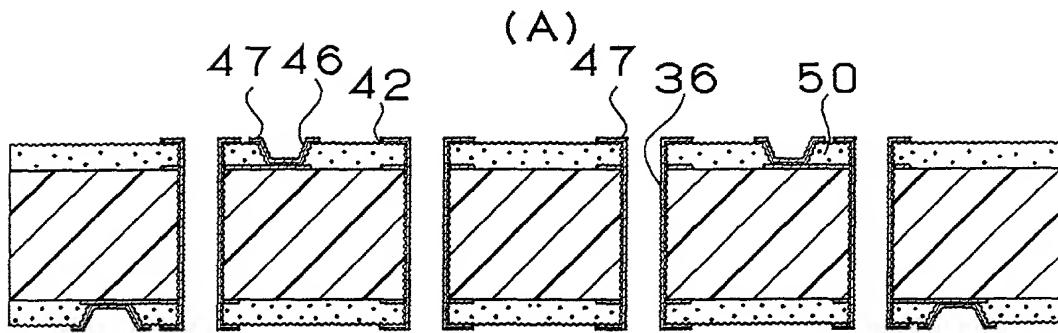
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Fig. 19/229



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Fig. 20



09/830963-02/06502

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Fig. 21

	roughing method	polishing of through hole land surface	flow of resin filler out of through holes
Comparison example 5	blackening-reduction process	No	Yes
Comparison example 6	etching	No	Yes
Comparison example 7	electroless plating	No	Yes
Second Embodiment	blackening-reduction process	Yes	No
First Modification of Second Embodiment	etching	Yes	No
Second Modification of Second Embodiment	electroless plating	yes	No

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Fig. 22

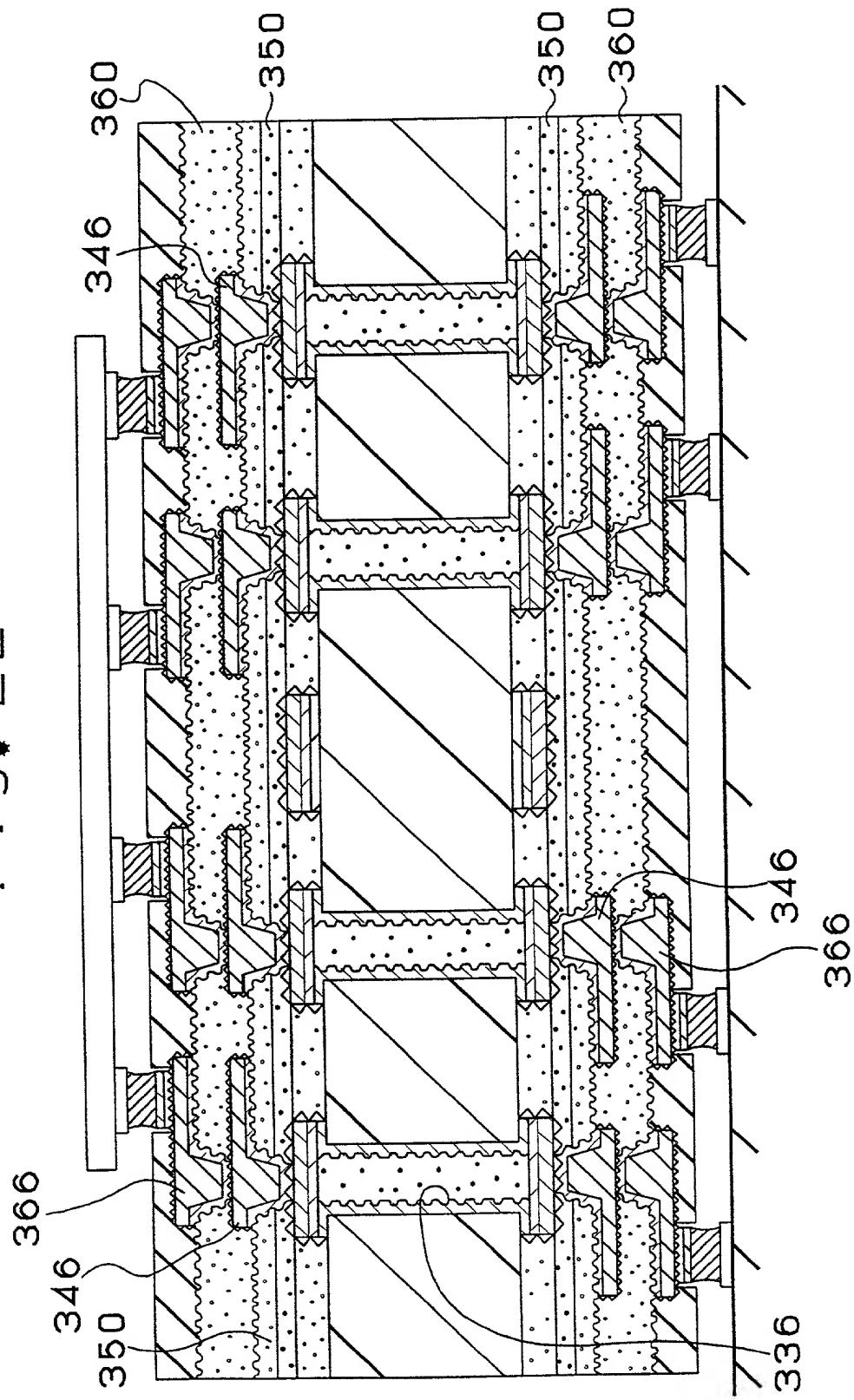


FIGURE 22 FIG. 22

FOR UTILITY/DESIGN
CIP/PCT NATIONAL/PLANT
ORIGINAL/SUBSTITUTE/SUPPLEMENTAL
DECLARATIONS

RULE 63 (37 C.F.R. 1.63)
DECLARATION AND POWER OF ATTORNEY
FOR PATENT APPLICATION
IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Pillsbury
Winthrop
FORM

As a below named inventor, I hereby declare that my residence, post office address and citizenship are as stated below next to my name, and I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the INVENTION ENTITLED Multi-Layer Printed Circuit Board And Method Of Manufacturing Multi-Layer Printed Circuit Board

the specification of which (CHECK applicable BOX(ES))

A. is attached hereto.
BOX(ES) → B. was filed on _____ as U.S. Application No. /
→ C. was filed as PCT International Application No. PCT/ JP00/07037 on October 10, 2000

and (if applicable to U.S. or PCT application) was amended on _____

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above. I acknowledge the duty to disclose all information known to me to be material to patentability as defined in 37 C.F.R. 1.56. Except as noted below, I hereby claim foreign priority benefits under 35 U.S.C. 119(a)-(d) or 365(b) of any foreign application(s) for patent or inventor's certificate, or 365(a) of any PCT International Application which designated at least one other country than the United States, listed below and have also identified below any foreign application for patent or inventor's certificate, or PCT International Application, filed by me or my assignee disclosing the subject matter claimed in this application and having a filing date (1) before that of the application on which priority is claimed, or (2) if no priority claimed, before the filing date of this application:

PRIOR FOREIGN APPLICATION(S)

<u>Number</u>	<u>Country</u>	<u>Day/MONTH/Year Filed</u>	<u>Date first Laid-open or Published</u>	<u>Date Patented or Granted</u>	<u>Priority NOT Claimed</u>
11-303305	Japan	26/October/1999			
11-303306	Japan	26/October/1999			
11-303307	Japan	26/October/1999			
2000-029988	Japan	08/February/2000			

If more prior foreign applications, X box at bottom and continue on attached page.

Except as noted below, I hereby claim domestic priority benefit under 35 U.S.C. 119(e) or 120 and/or 365(c) of the indicated United States applications listed below and PCT international applications listed above or below and, if this is a continuation-in-part (CIP) application, insofar as the subject matter disclosed and claimed in this application is in addition to that disclosed in such prior applications, I acknowledge the duty to disclose all information known to me to be material to patentability as defined in 37 C.F.R. 1.56 which became available between the filing date of each such prior application and the national or PCT international filing date of this application:

PRIOR U.S. PROVISIONAL, NONPROVISIONAL AND/OR PCT APPLICATION(S)

<u>Application No. (series code/serial no.)</u>	<u>Day/MONTH/Year Filed</u>	<u>Status</u>	<u>Priority NOT Claimed</u>
		<u>pending, abandoned, patented</u>	

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true, and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

And I hereby appoint Pillsbury Winthrop LLP, Intellectual Property Group, 1100 New York Avenue, N.W., Ninth Floor, East Tower, Washington, D.C. 20005-3918, telephone number (202) 861-3000 (to whom all communications are to be directed), and the below-named persons (of the same address) individually and collectively my attorneys to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith and with the resulting patent, and I hereby authorize them to delete names/numbers below of persons no longer with their firm and to act and rely on instructions from and communicate directly with the person/assignee/attorney/firm/ organization who/which first sends/sent this case to them and by whom/which I hereby declare that I have consented after full disclosure to be represented unless/until I instruct the above Firm and/or a below attorney in writing to the contrary.

Paul N. Kokulis 16773

Glenn J. Perry	<u>28458</u>	Stephen C. Glazier	<u>31361</u>	William P. Atkins	<u>38821</u>
				Paul L. Sharer	<u>36004</u>
Kevin E. Joyce	<u>20508</u>	Richard H. Zaitlen	<u>27248</u>	Robin L. Teskin	<u>35030</u>
George M. Sirilla	<u>18221</u>	Roger R. Wise	<u>31204</u>		
Donald J. Bird	<u>25323</u>	Michael R. Dzwonczyk	<u>36787</u>		
Dale S. Lazar	<u>28872</u>	W. Patrick Bengtsson	<u>32456</u>		
		Jack S. Barufka	<u>37087</u>		
		Adam R. Hess	<u>41835</u>		

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Date: 2001/4/26

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Date: 2001/4/26

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(include Zip Code) <u>503-0961</u>		

"X" box FOR ADDITIONAL INVENTORS, and proceed on the attached page to list each additional inventor.

See additional foreign priorities on attached page (incorporated herein by reference).

Atty. Dkt. No. PM
(M#)

Rule 56(a) & (b) = 37 C.F.R. 1.56(a) & (b)
PATENT AND TRADEMARK CASES - RULES OF PRACTICE
DUTY OF DISCLOSURE

(a) ... Each individual associated with the filing and prosecution of a patent application has a duty of candor and good faith in dealing with the [Patent and Trademark] Office, which includes a duty to disclose to the Office all information known to that individual to be material to patentability... (b) information is material to patentability when it is not cumulative and (1) It also establishes by itself, or in combination with other information, a prima facie case of unpatentability of a claim or (2) refutes, or is inconsistent with, a position the applicant takes in: (i) Opposing an argument of unpatentability relied on by the Office, or (ii) Asserting an argument of patentability

PATENT LAWS 35 U.S.C.

§102. Conditions for patentability; novelty and loss of right to patent

A person shall be entitled to a patent unless--

(a) the invention was known or used by others in this country, or patented or described in a printed publication in this or a foreign country, before the invention thereof by the applicant for patent or

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of the application for patent in the United States, or

(c) he has abandoned the invention, or

(d) the invention was first patented or caused to be patented, or was the subject of an inventor's certificate, by the applicant or his legal representatives or assigns in a foreign country prior to the date of the application for patent in this country on an application for patent or inventor's certificate filed more than twelve months* before the filing of the application in the United States, or

(e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent, or

(f) he did not himself invent the subject matter sought to be patented, or

(g) before the applicant's invention thereof the invention was made in this country by another who had not abandoned, suppressed, or concealed it. In determining priority of invention there shall be considered not only the respective dates of conception and reduction to practice of the invention, but also the reasonable diligence of one who was first to conceive and last to reduce to practice, from a time prior to conception by the other.

§103. Condition for patentability; non-obvious subject matter

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made. . . .

(c) Subject matter developed by another person, which qualified as prior art only under subsection (f) or (g) of section 102 of this title, shall not preclude patentability under this section where the subject matter and the claimed invention were, at the time the invention was made, owned by the same person or subject to an obligation of assignment to the same person.

* Six months for Design Applications (35 U.S.C. 172).

DECLARATION AND POWER OF ATTORNEY

(continued)

ADDITIONAL INVENTORS:

(3) INVENTOR'S SIGNATURE:

Yutaka Iwata

Date: 2001.4.26

(3) INVENTOR'S SIGNATURE:		Yutaka Iwata		IWATA	
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Residence	Ogaki	Japan	JPX	Japan	
		City	State/Foreign Country		Country of Citizenship
Mailing Address	c/o Aoyagi-kojou, IBIDEN Co., Ltd. 300, Aoyagicho, Ogaki-shi, Gifu Japan				
(include Zip Code)	503-0961				

(4) INVENTOR'S SIGNATURE: Tetsuya Tanabe

Date: 2001-4-26

(4) INVENTOR'S SIGNATURE:		Tetsuya Tanabe		TANABE	
		First	Middle Initial	Family Name	
Residence	Ogaki	Japan	JPX	Japan	
		City	State/Foreign Country		Country of Citizenship
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(include Zip Code)	503-0961				